

General Description

The LTA8081, LTA8082 and LTA8084 (LTA808x) are a family of low power, 48 V wide supply voltage, rail-to-rail output, precision operational amplifiers capable of operating on supplies ranging from +4.5 V (± 2.25 V) to +48 V (± 24 V). This new generation of high-voltage CMOS operational amplifiers, in conjunction with the LTA809x, LTA807x and LTA806x, provide a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications. The LTA808x devices offer outstanding dc precision and ac performance, including low offset (± 75 μ V typically), low offset drift (± 1.5 μ V/ $^{\circ}$ C typically), 10 MHz bandwidth, and 8 nV/ \sqrt Hz input voltage noise density at 10 kHz. Unique features such as differential input-voltage range to the negative supply rail, high output current (± 45 mA), high capacitive load drive of up to 1 nF, and high slew rate (9 V/ μ s) make the LTA808x high-performance operational amplifiers for high-voltage industrial applications.

The robust design of the LTA808x family provides ease-of-use to the circuit designer: integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection. The LTA808x are optimized for operation at voltages from +4.5 V (± 2.25 V) to +48 V (± 24 V) over the extended temperature range of -40 $^{\circ}$ C to $+125$ $^{\circ}$ C.

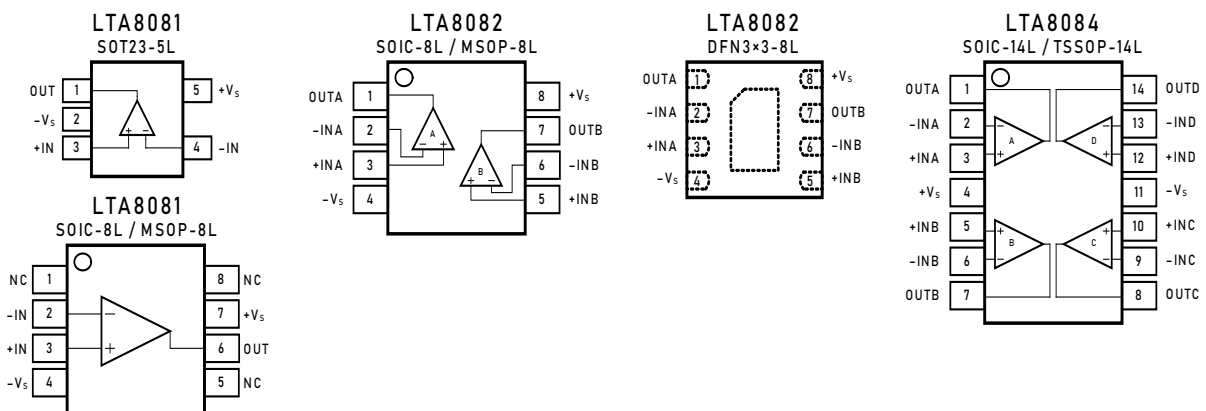
Features and Benefits

- Wide Supply: ± 2.25 V to ± 24 V, 4.5 V to 48 V
- Low Offset Voltage: ± 75 μ V Typically
- Low Offset Voltage Drift: ± 1.5 μ V/ $^{\circ}$ C
- High Common-Mode Rejection: 116 dB
- Gain Bandwidth: 10 MHz
- Slew Rate: 9 V/ μ s
- Low Noise: 8 nV/ \sqrt Hz at 10 kHz
- Low Bias Current: ± 10 pA
- Rail-to-Rail Output

Applications

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- High-Side and Low-Side Current Sensing
- High Precision Comparator
- Battery-Powered Instruments
- Test and Measurement Equipment
- Multiplexed Data-Acquisition Systems
- Programmable Logic Controllers

Pin Configuration (Top View)



Pin Description

Symbol	Description
-IN	Inverting input of the amplifier. The voltage range is from V_{S-} to $V_{S+} - 1.5$ V.
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as -IN.
+ V_S	Positive power supply. The voltage is from 4.5 V to 48 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 4.5 V to 48 V.
- V_S	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 4.5 V to 48 V.
OUT	Amplifier output.
NC	No connection

Ordering Information ⁽¹⁾

Type Number	Package Name	Package Quantity	Eco Class ⁽²⁾	Marking Code ⁽³⁾
LTA8081XT5/R6	SOT23-5L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	H81
LTA8081XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	HV-81
LTA8081XV8/R6	MSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	HV81
LTA8082XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	HV-82
LTA8082XV8/R6	MSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	HV82
LTA8082XF8/R10	DFN3x3-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	HV82
LTA8084XS14/R5	SOIC-14L	Tape and Reel, 2 500	Green (RoHS & no Sb/Br)	HV-84
LTA8084XT14/R6	TSSOP-14L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	HV-84

- (1) Please contact to your Linearin representative for the latest availability information and product content details.
 (2) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).
 (3) There may be multiple device markings, a varied marking character of "x", or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Limiting Value - In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	60 V
Signal Input Terminals: Voltage, Current	$-V_S - 0.3$ V to $+V_S + 0.3$ V, ± 10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	-65 to $+150$ °C
Junction Temperature, T_J	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9 ⁽¹⁾	2 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014 ⁽²⁾	2 000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

Electrical Characteristics

$V_S = 4.5 \text{ V to } 48 \text{ V}$, $T_A = +25 \text{ }^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, unless otherwise noted. Boldface limits apply over the specified temperature range, $T_A = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}$.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			± 75	± 350	μV
Offset voltage drift	$V_{OS \text{ TC}}$	$T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$		± 1.5		$\mu\text{V}/^\circ\text{C}$
Power supply rejection ratio	PSRR	$V_S = 4.5 \text{ to } 48 \text{ V}$, $V_{CM} = 0.1 \text{ V}$		3.5		$\mu\text{V}/\text{V}$
		$T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$		10		
INPUT BIAS CURRENT						
Input bias current	I_B			10		pA
		$T_A = +85 \text{ }^\circ\text{C}$		150		
		$T_A = +125 \text{ }^\circ\text{C}$		600		
Input offset current	I_{OS}			5		pA
NOISE						
Input voltage noise	V_n	$f = 0.1 \text{ to } 10 \text{ Hz}$		4		μV_{P-P}
Input voltage noise density	e_n	$f = 1 \text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10 \text{ kHz}$		8		
Input current noise density	I_n	$f = 1 \text{ kHz}$		5		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}		$-V_S$		$+V_S - 1.5$	V
Common-mode rejection ratio	CMRR	$V_S = 40 \text{ V}$, $V_{CM} = 0 \text{ to } 38 \text{ V}$		116		dB
		$V_{CM} = 0.1 \text{ to } 38 \text{ V}$, $T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$		103		
		$V_S = 5 \text{ V}$, $V_{CM} = 0 \text{ to } 3.5 \text{ V}$		96		
		$V_{CM} = 0.1 \text{ to } 3 \text{ V}$, $T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$		84		
INPUT IMPEDANCE						
Input capacitance	C_{IN}	Differential		2		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{VOL}	$V_S = 40 \text{ V}$, $V_O = 0.1 \text{ to } 39.9 \text{ V}$		130		dB
		$T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$		120		
		$V_S = 5 \text{ V}$, $V_O = 0.1 \text{ to } 4.9 \text{ V}$		122		
		$T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$		112		
FREQUENCY RESPONSE						
Gain bandwidth product	GBW			10		MHz
Slew rate	SR	$V_S = 40 \text{ V}$, $G = +1$, 10 V step		9		$\text{V}/\mu\text{s}$
Total harmonic distortion + noise	THD+N	$G = +1$, $f = 1 \text{ kHz}$, $V_O = 3 V_{RMS}$		0.0002		%
Settling time	t_S	To 0.1%, $V_S = 40 \text{ V}$, $G = +1$, 5 V step		1.6		μs
		To 0.01%, $V_S = 40 \text{ V}$, $G = +1$, 5 V step		3.5		
Overload recovery time	t_{OR}	$V_{IN} \times \text{Gain} > V_S$		0.6		μs

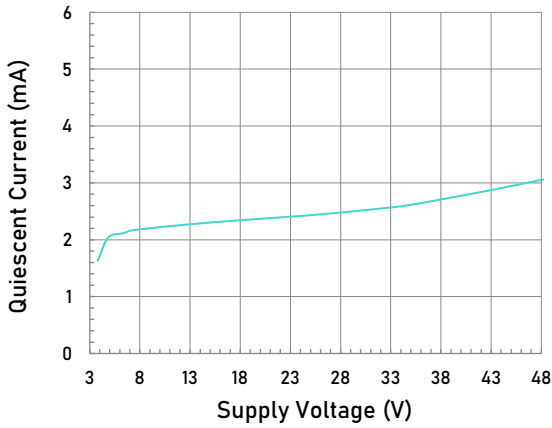
Electrical Characteristics (continued)

$V_S = 4\text{ V to }48\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, unless otherwise noted. Boldface limits apply over the specified temperature range, $T_A = -40\text{ }^\circ\text{C to }+125\text{ }^\circ\text{C}$.

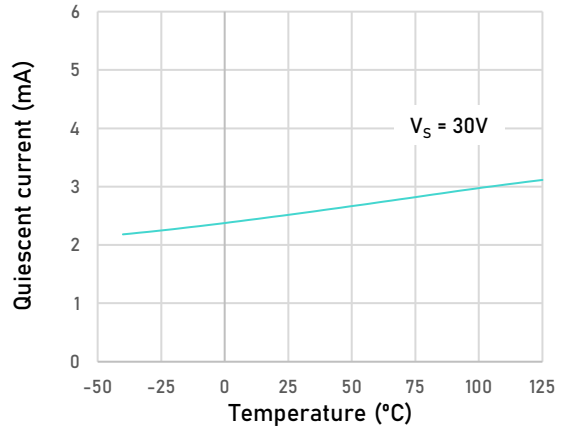
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<i>OUTPUT</i>						
High output voltage swing	V_{OH}	$V_S = \pm 20\text{ V}$, $R_L = 10\text{ k}\Omega$		$+V_S - 95$		mV
		$V_S = \pm 20\text{ V}$, $R_L = 2\text{ k}\Omega$		$+V_S - 255$		
Low output voltage swing	V_{OL}	$V_S = \pm 20\text{ V}$, $R_L = 10\text{ k}\Omega$		$-V_S + 60$		mV
		$V_S = \pm 20\text{ V}$, $R_L = 2\text{ k}\Omega$		$-V_S + 240$		
Short-circuit current	I_{SC}			± 45		mA
<i>POWER SUPPLY</i>						
Operating supply voltage	V_S	$T_A = -40\text{ to }+125\text{ }^\circ\text{C}$	4.5		48	V
Quiescent current (per amplifier)	I_Q	$V_S = 5\text{ V}$		2.05		mA
		$V_S = 40\text{ V}$		2.75		
<i>THERMAL CHARACTERISTICS</i>						
Operating temperature range	T_A		-40		+125	$^\circ\text{C}$
Package Thermal Resistance	θ_{JA}	SOT23-5L		190		$^\circ\text{C/W}$
		MSOP-8L		201		
		SOIC-8L		125		
		TSSOP-14L		112		
		SOIC-14L		115		

Typical Performance Characteristics

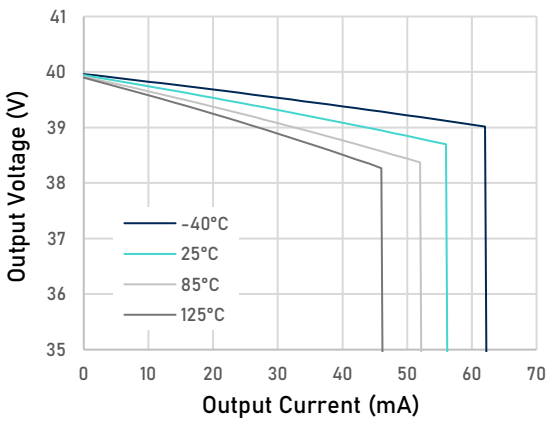
At $T_A = +25^\circ\text{C}$, $V_{CM} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, unless otherwise noted.



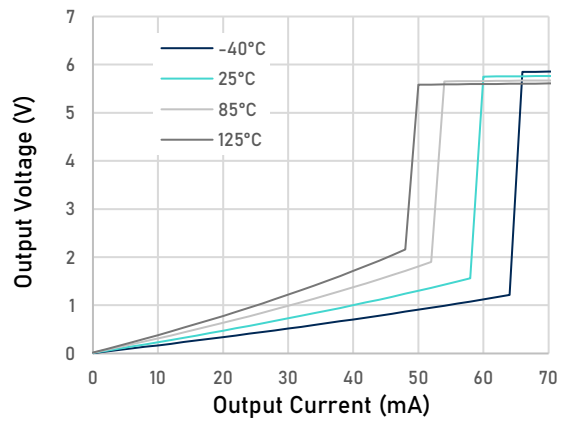
Quiescent Current as a function of Supply Voltage



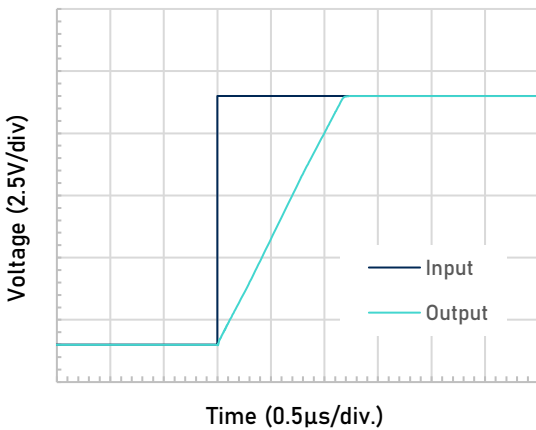
Quiescent Current as a function of Temperature



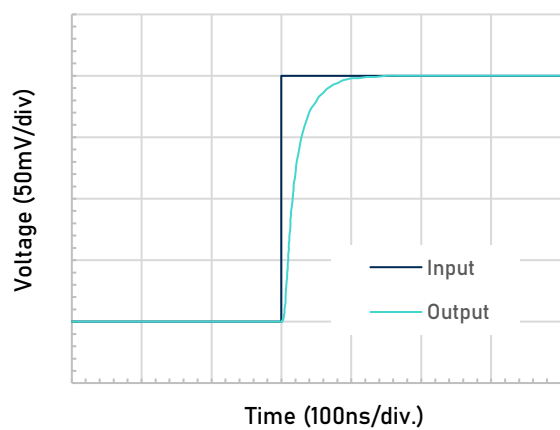
Output Voltage Swing as a function of Output Current (Sourcing, $V_S = 40\text{ V}$)



Output Voltage Swing as a function of Output Current (Sinking, $V_S = 40\text{ V}$)



Large-Signal Step Response(Failing)

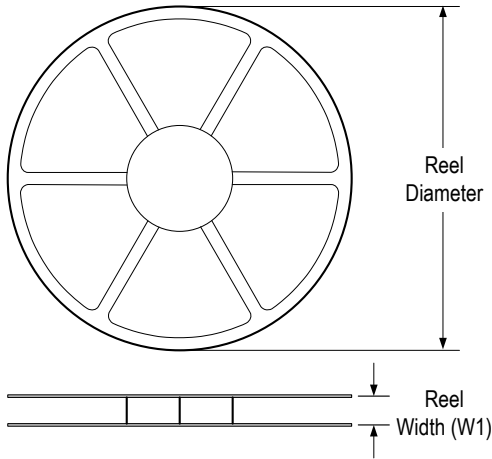


Small-Signal Step Response

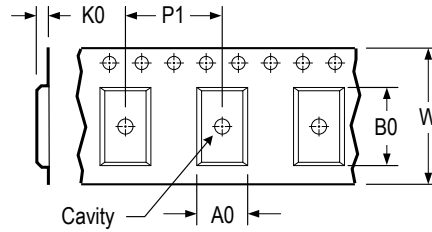
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Tape and Reel Information

REEL DIMENSIONS

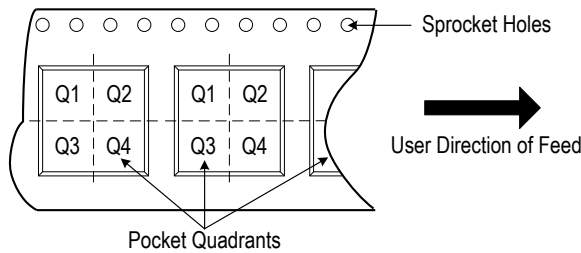


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

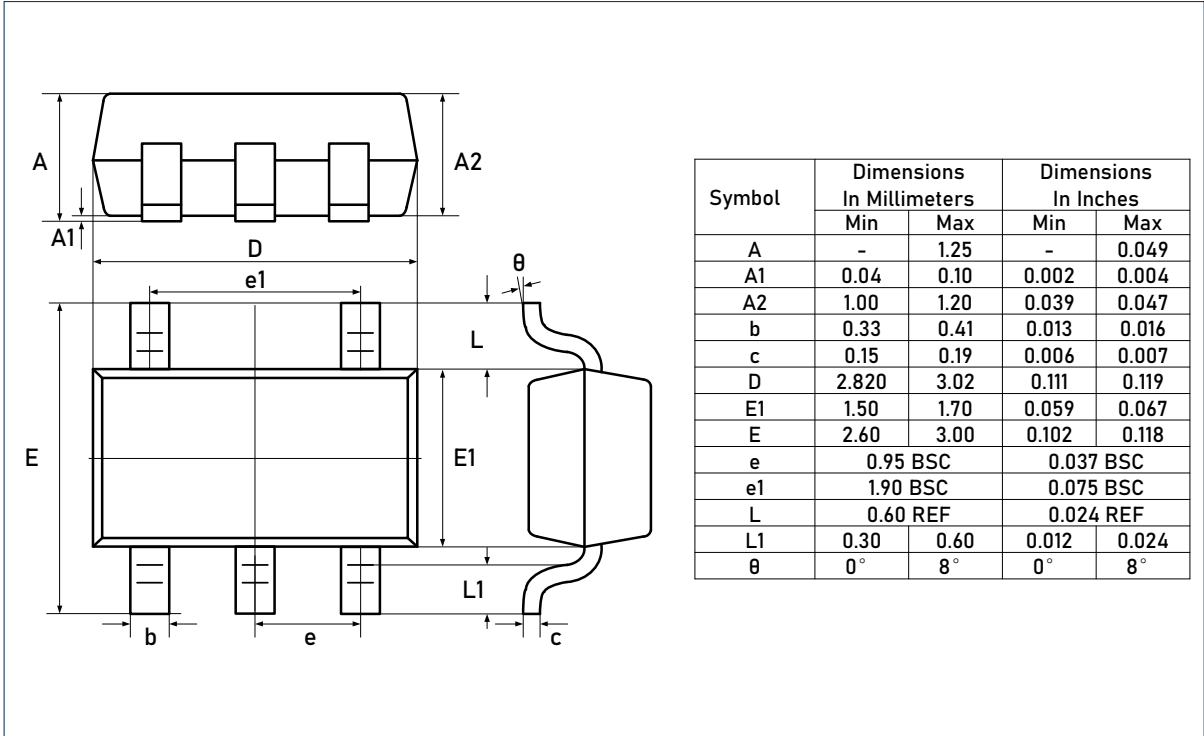


* All dimensions are nominal

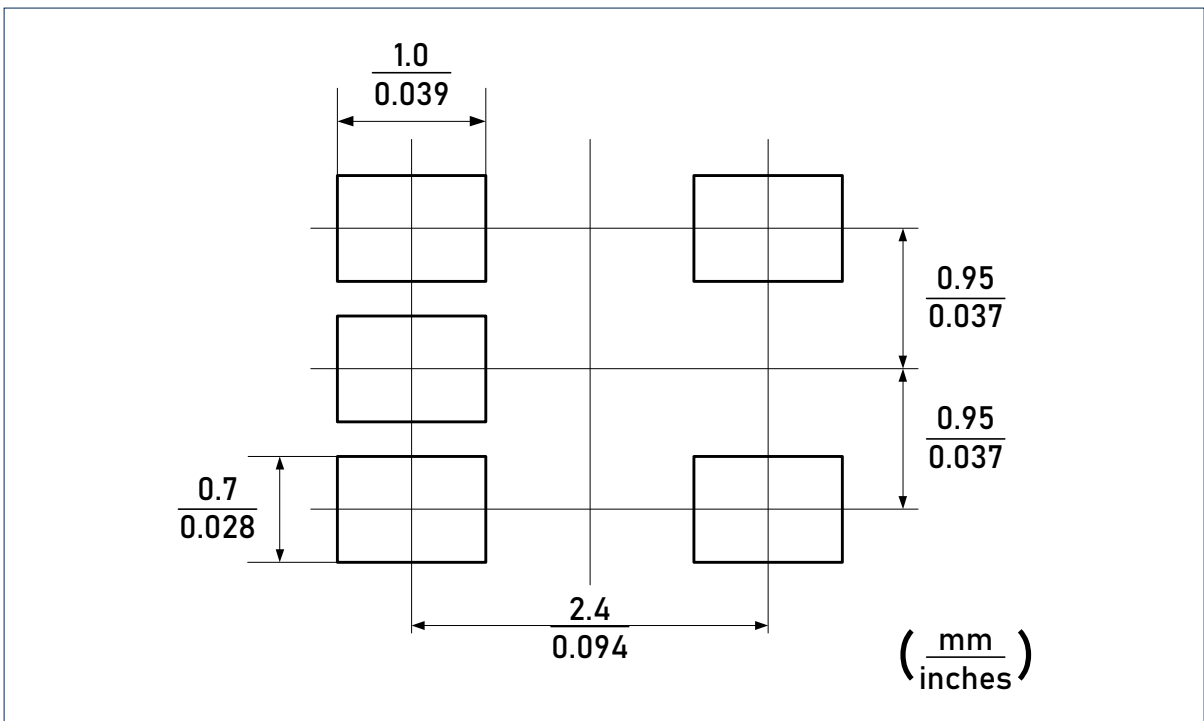
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA8081XT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

Package Outlines

DIMENSIONS, SOT23-5L



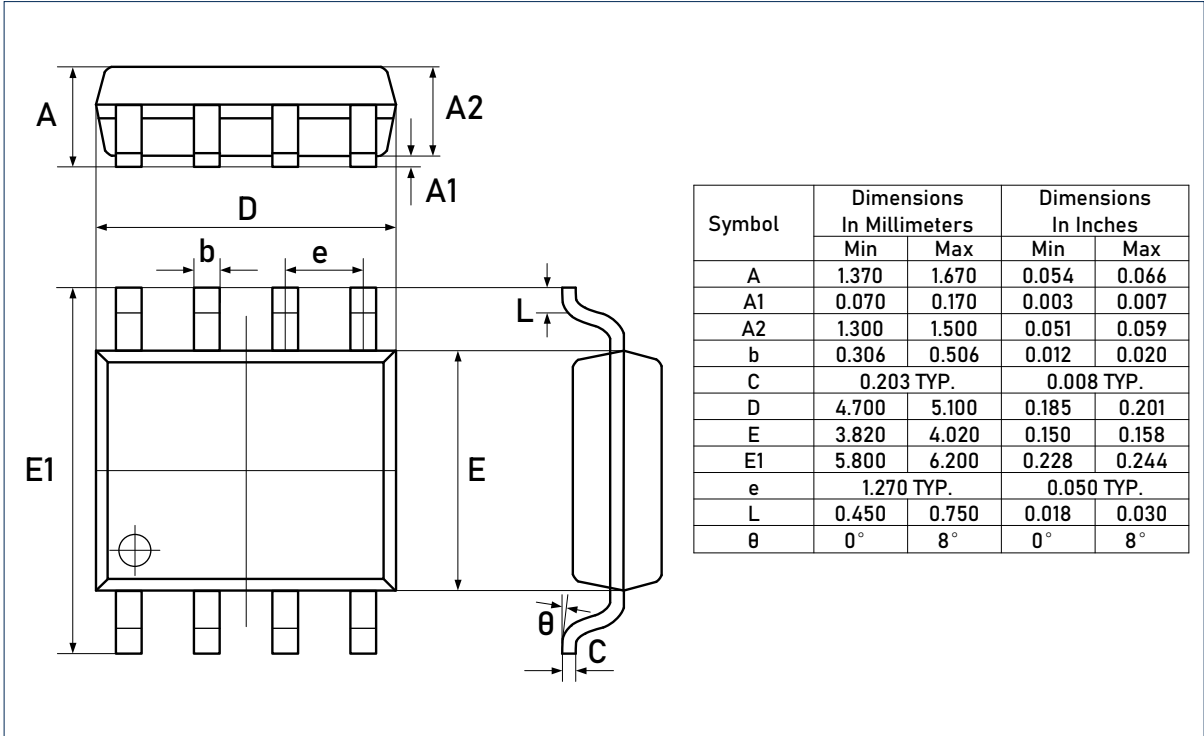
RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



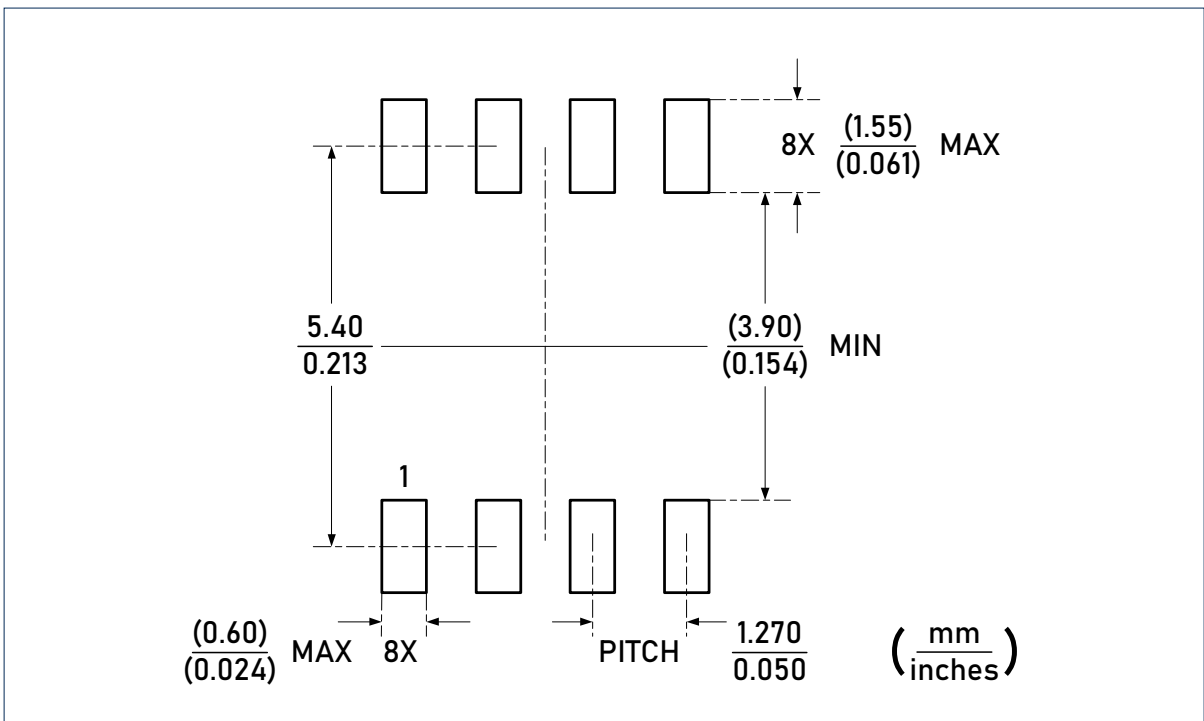
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Package Outlines (continued)

DIMENSIONS, SOIC-8L



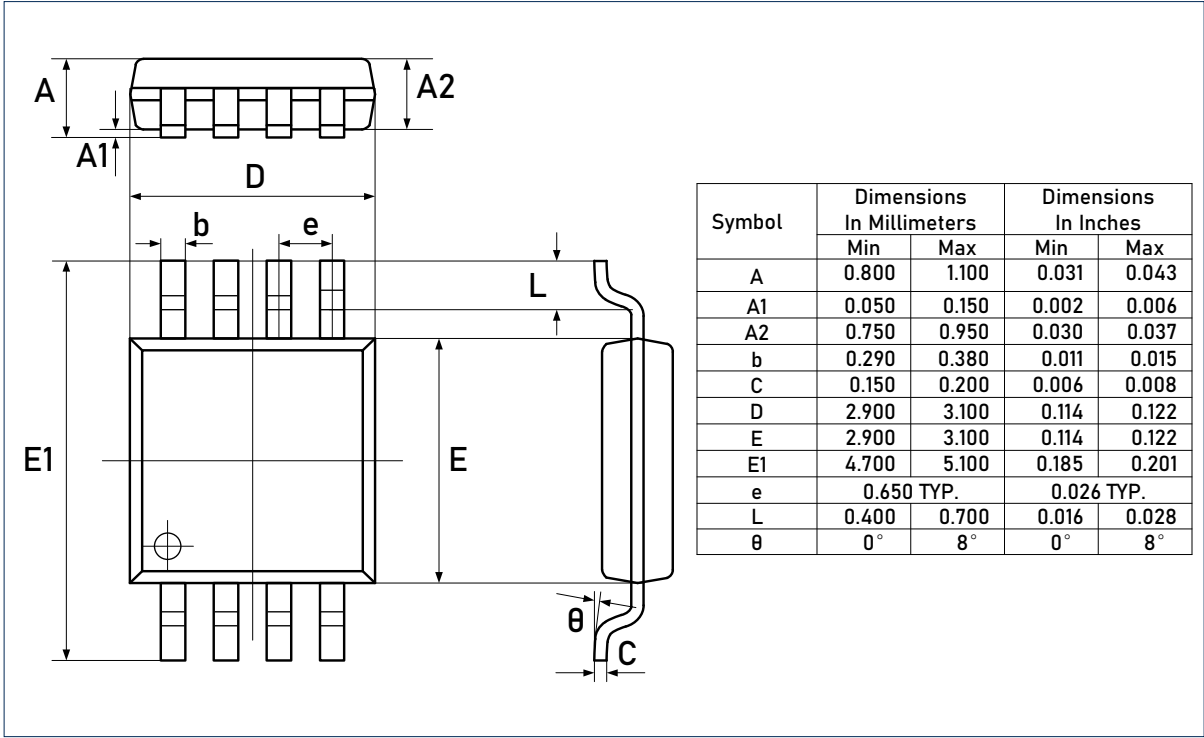
RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



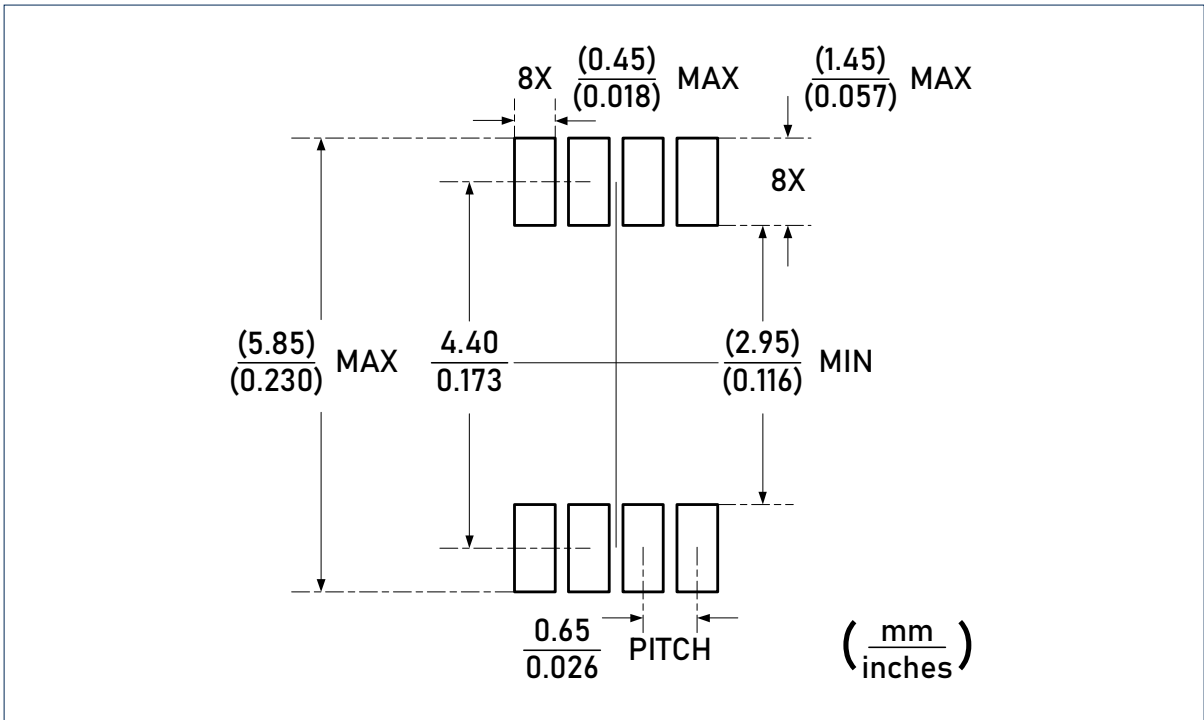
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Package Outlines (continued)

DIMENSIONS, MSOP-8L



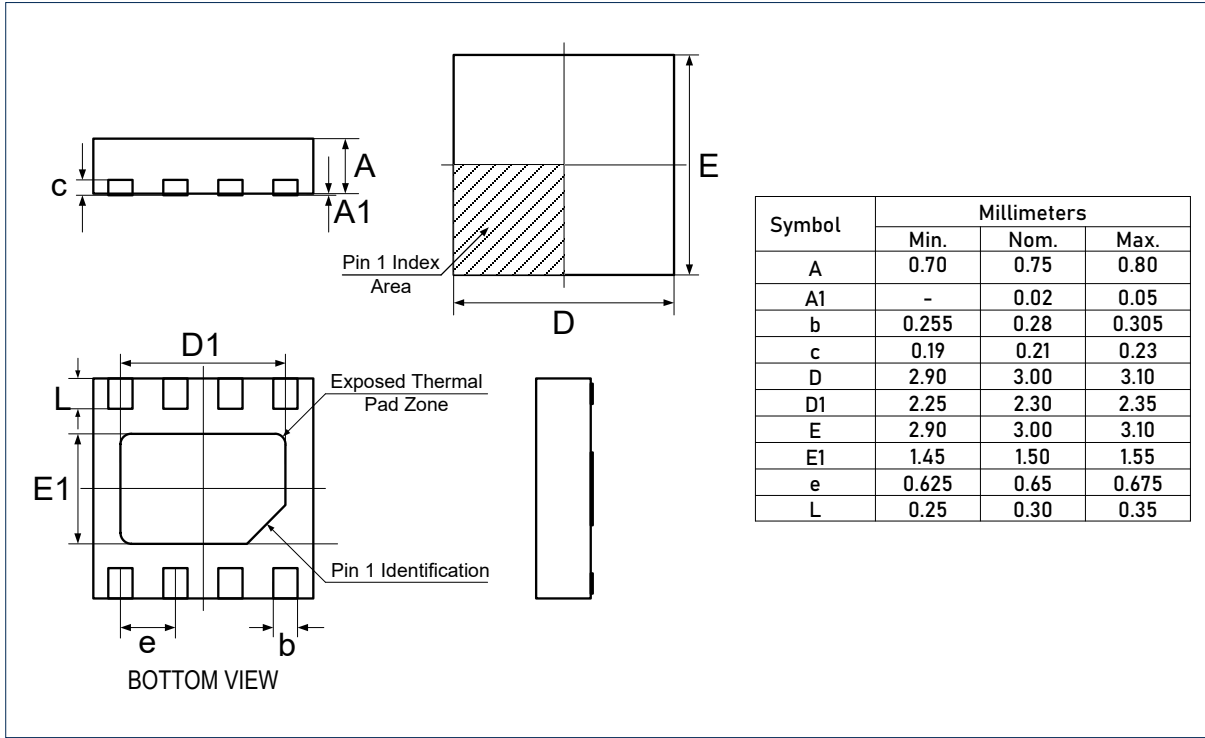
RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



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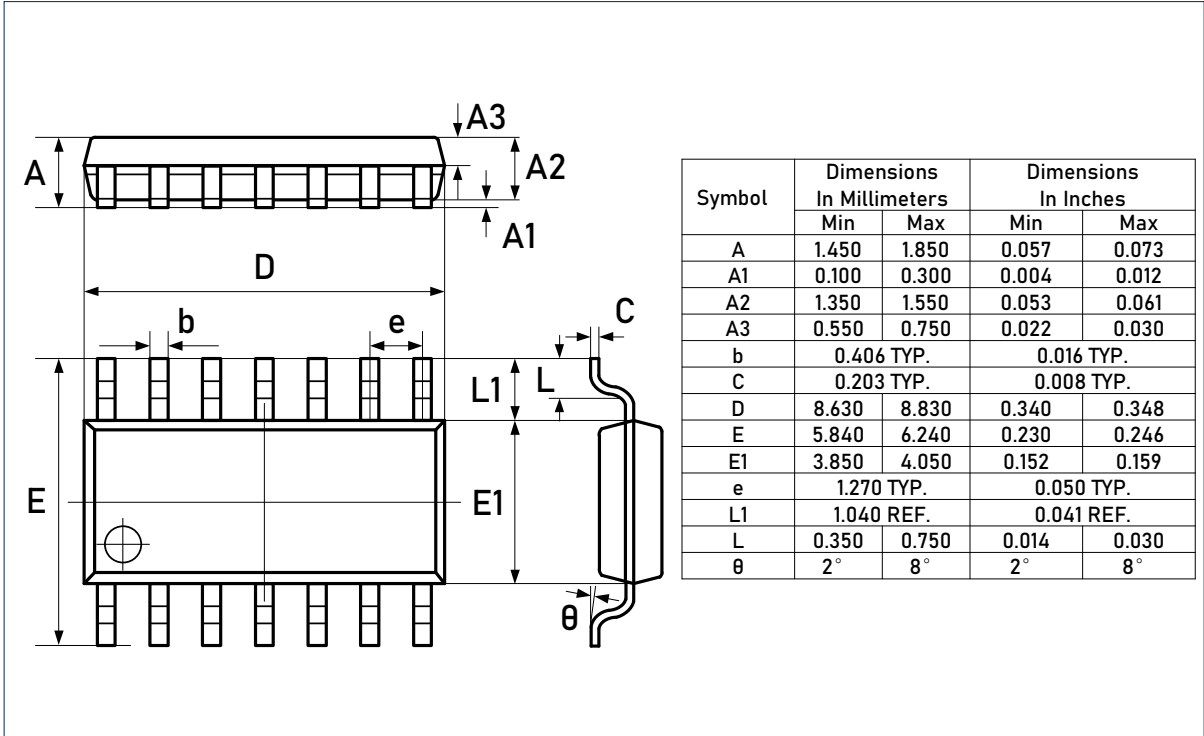
Package Outlines (continued)

DIMENSIONS, DFN3x3-8L

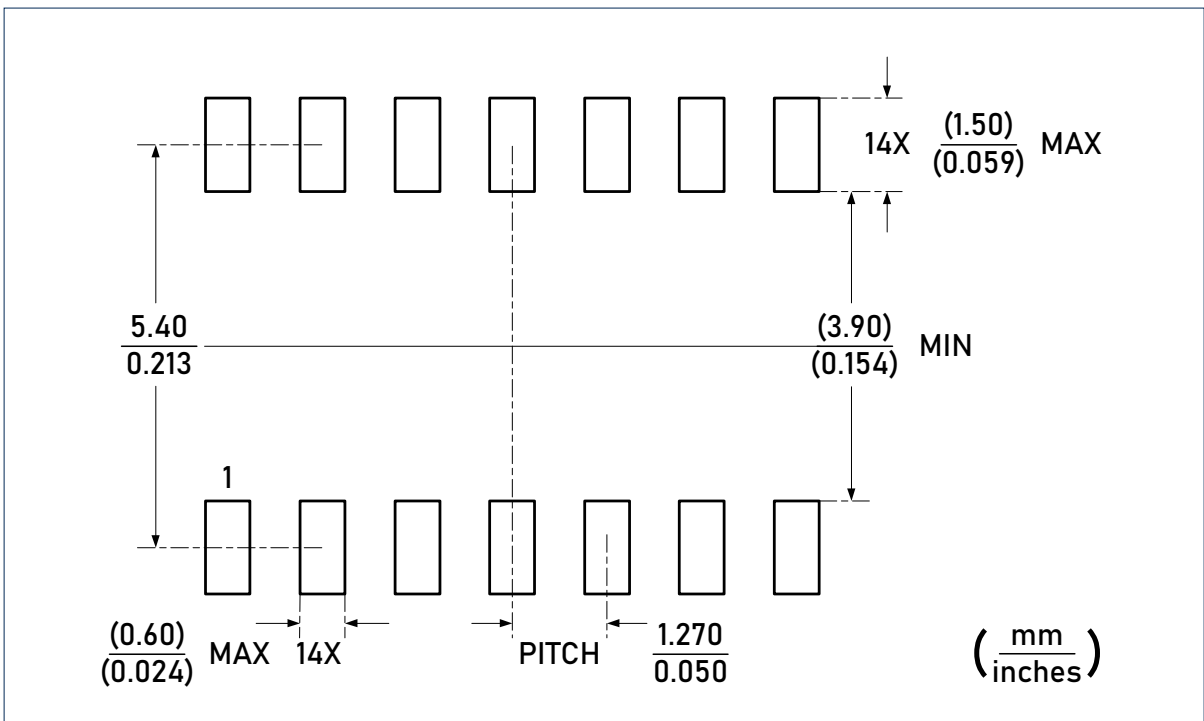


Package Outlines (continued)

DIMENSIONS, SOIC-14L



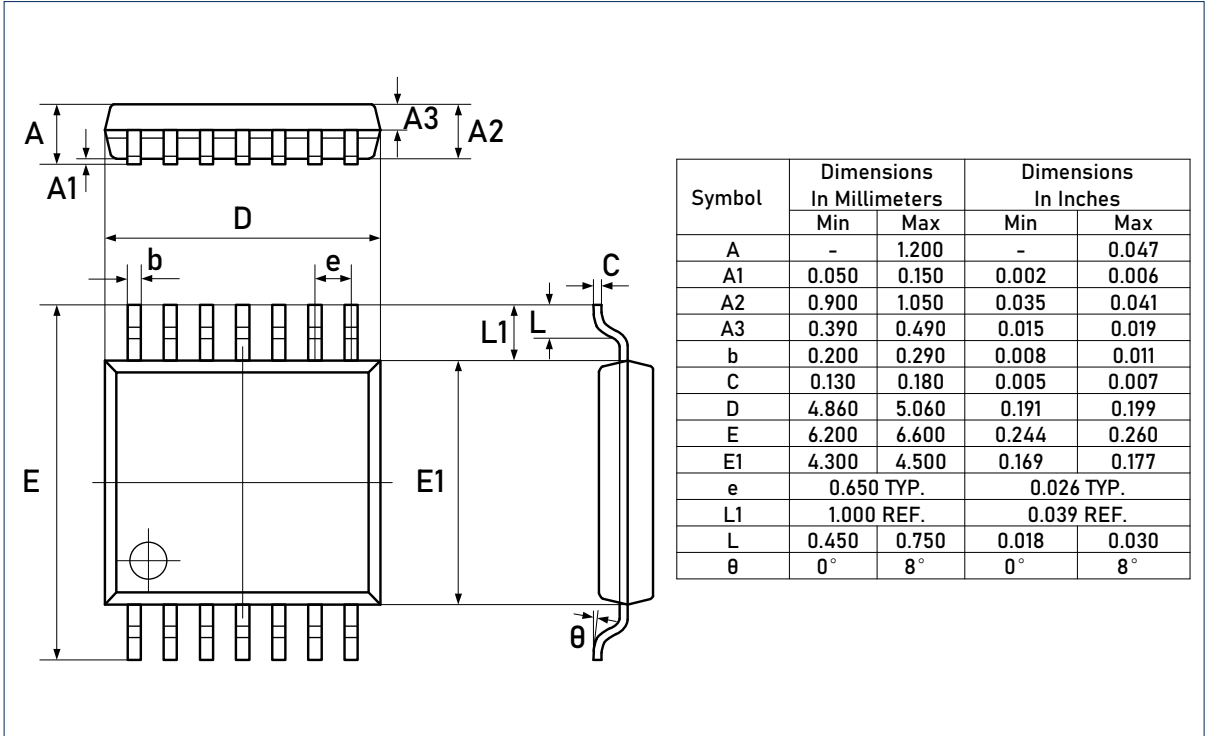
RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



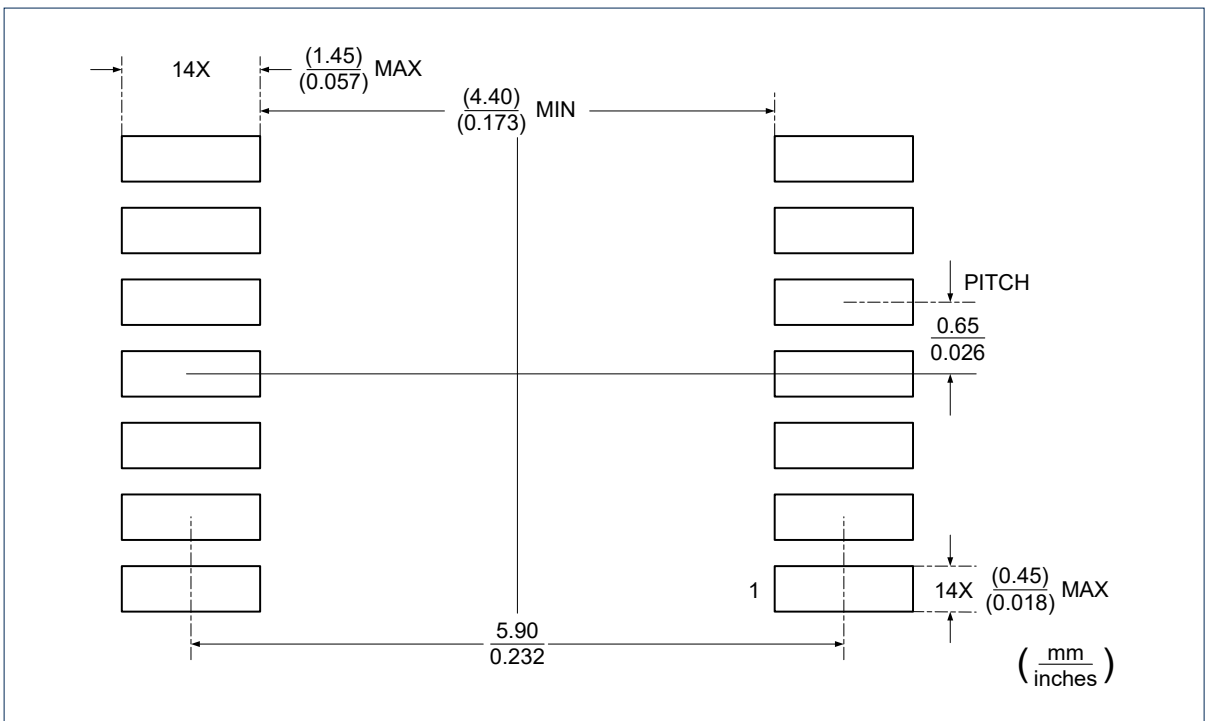
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Package Outlines (continued)

DIMENSIONS, TSSOP-14L



RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



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Important Notice

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