

General Description

The LTA321/LTA323/LTA2904/LTA2902 are single-, dual-, quad- channel amplifiers that feature 300 μ A quiescent current per Amplifier, a wide range of supply voltages from 3 V to 36 V helps to implement in a wide variety of applications where require critical response time, power-sensitive, high-voltage. It also provides low offset (± 3 mV), Wide CMVR (Common-mode voltage range) from V_{s-} to $V_{s+} - 1.5$ V, 105 dB high Open-loop voltage gain. 40 mA current output and high slew rate (0.98 V/ μ s) make LTA321/LTA323/LTA2904/LTA2902 very suitable for high voltage industrial applications.

The LTA321 and LTA323 (Single) is available in SOT23-5L package. The LTA2904 (Dual) is offered in TSSOP-8L, SOIC-8L and MSOP-8L packages, The LTA2902 (Quad) is offered in SOIC-14L, TSSOP-14L and DIP-14L packages. All devices are rated over -40°C to $+125^{\circ}\text{C}$ extended industrial temperature range.

Features and Benefits

- 3 V to 36 V Single supply or ± 1.5 V to ± 18 V Dual supply
- Low quiescent current: 300 μ A / Amplifier
- Gain Bandwidth: 1.3 MHz
- Slew Rate: 0.98 V/ μ s
- Very Low Noise: 20 nV / $\sqrt{\text{Hz}}$ at 1kHz
- Common-mode input voltage range includes V_{s-}
- Low offset voltage: ± 3 mV
- -40°C to 125°C Operation temperature
- Rail-to-Rail Output
- Drop in replacement with 2904, 2902 family products

Applications

- Industrial Application
- Solar Inverter
- White Goods
- Battery Management System
- Power supplies

Table of Content

General Description.....	1
Features and Benefits.....	1
Applications.....	1
Table of Content	2
Revision History	2
Ordering Information ⁽¹⁾	3
Pin Configuration (Top View)	3
Limiting Value– In accordance with the Absolute Maximum Rating System (IEC 60134)	6
ESD Ratings	6
Thermal Information.....	6
Electrical Characteristics.....	7
Typical Characteristics.....	8
Detailed Description.....	10
Typical Application Circuits	11
Tape and Reel Information.....	12
Package Outlines	13
Important Notice	20

Revision History

Version FN1624-29.0 (Jul,2024)

- Initial version.

Ordering Information⁽¹⁾

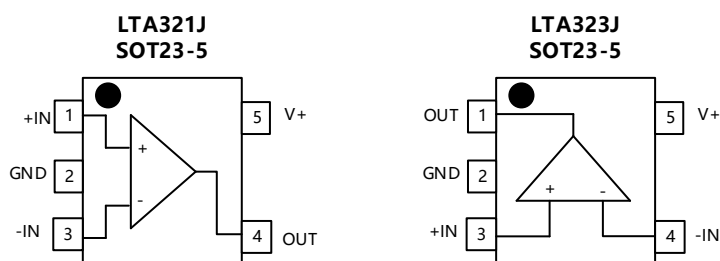
Part Number	Package Type	Quantity	ECO Class ⁽²⁾	Mark Code ⁽³⁾
LTA321JXT5/R6	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	G21
LTA323JXT5/R6	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	G23
LTA2904XS8/R8	SOIC-8L	4 000	Green (RoHS & no Sb/Br)	G2904
LTA2904XV8/R6	MSOP-8L	3 000	Green (RoHS & no Sb/Br)	G2904
LTA2904XT8/R6	TSSOP-8L	3 000	Green (RoHS & no Sb/Br)	G2904
LTA2902XS14/R5	SOIC-14L	2 500	Green (RoHS & no Sb/Br)	G2902
LTA2902XT14/R6	TSSOP-14L	3 000	Green (RoHS & no Sb/Br)	G2902
LTA2902XD14/R2	DIP-14L	1 000	Green (RoHS & no Sb/Br)	G2902

(1) Please contact to your Linearin representative for the latest availability information and product content details.

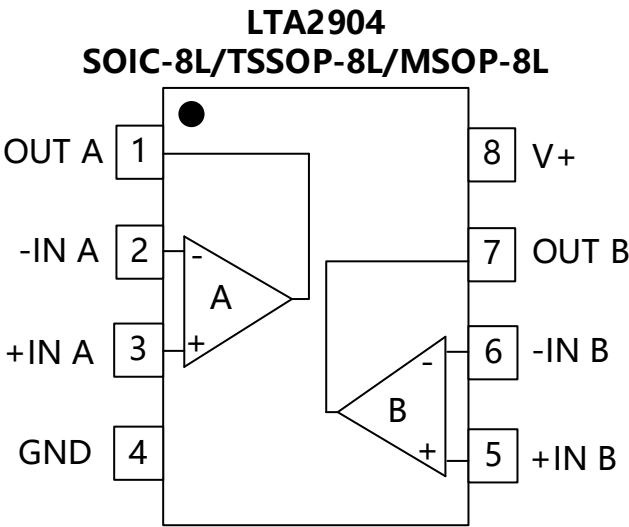
(2) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).

(3) There may be multiple device markings, a varied marking character of "x", or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

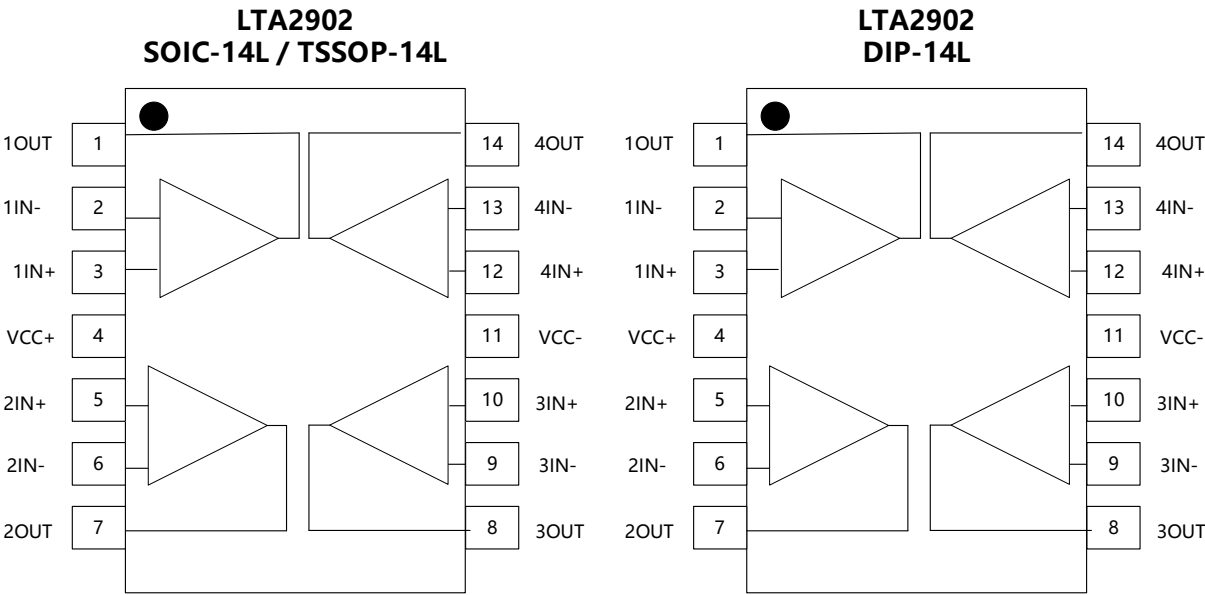
Pin Configuration (Top View)



Symbol	LTA321J	LTA323J	Description
	SOT23-5L		
-IN	3	4	Inverting input
+IN	1	3	Non-inverting input
OUT	4	1	Output
GND	2	2	Ground
V+	5	5	Positive power supply



Symbol	LTA2904	Description
	SOIC-8L/MSOP8/TSSOP-8	
-IN A	2	Inverting input, channel A
+IN A	3	Non-inverting input, channel A
-IN B	6	Inverting input, channel B
+IN B	5	Non-inverting input, channel B
OUT A	1	Output, channel A
OUT B	7	Output, channel B
GND	4	Ground
V+	8	Positive power supply



Symbol	LTA2902	Description
	SOIC-14L / TSSOP-14L/PDIP-14L	
1 IN-	2	Inverting input, channel 1
1 IN+	3	Non-inverting input, channel 1
1 OUT	1	Output, channel 1
GND	11	Ground
2 IN-	6	Inverting input, channel 2
2 IN+	5	Non-inverting input, channel 2
2 OUT	7	Output, channel 2
V+	4	Positive power supply
3 IN-	9	Inverting input, channel 3
3 IN+	10	Non-inverting input, channel 3
3 OUT	8	Output, channel 3
4 IN-	13	Inverting input, channel 4
4 IN+	12	Non-inverting input, channel 4
4 OUT	14	Output, channel 4

Limiting Value– In accordance with the Absolute Maximum Rating System (IEC 60134)

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	± 20 V
Differential input voltage ⁽¹⁾	± 20 V
Input voltage range (either input)	± 20 V
Input current	40 mA
Storage Temperature Range, T_{sta}	-65°C to $+150^{\circ}\text{C}$
Junction Temperature, T_j	150°C

(1) The differential input voltage is the value on IN+ with respect to IN–.

ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	5 000	V
Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	2 000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

Thermal Information

Thermal Metric		Package		Unit
θ_{JA}	Thermal Resistance	SOT23-5L	190	$^{\circ}\text{C}/\text{W}$
		SOIC-8L	125	
		TSSOP-8L	160	
		MSOP-8L	201	
		SOIC-14L	115	
		TSSOP-14L	112	
		DIP-14L	65	

Electrical Characteristics

At $T_A = 25^\circ\text{C}$ and $V_S = +5\text{ V}$ to $+36\text{ V}$, $V_{CM} = V_{out} = V_S/2$, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$T_A = -40$ to $+125^\circ\text{C}$		± 0.5	± 3	mV
					± 4	
$V_{OS\ TC}$	Offset voltage drift	$T_A = -40$ to $+125^\circ\text{C}$		± 6		$\mu\text{V}/^\circ\text{C}$
$PSRR$	Power supply rejection ratio	$T_A = -40$ to $+125^\circ\text{C}$	90	105		dB
				102		
INPUT BIAS CURRENT						
I_B	Input bias current	$T_A = -40$ to $+125^\circ\text{C}$		20		nA
				40		
I_{OS}	Input offset current	$T_A = -40$ to $+125^\circ\text{C}$		5		nA
				10		
NOISE						
V_n	Input voltage noise	$f = 0.1$ to 10 Hz		4.5		μV_{P-P}
e_n	Input voltage noise density	$f = 1\text{ kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		V_{S-}		$V_{S+} - 1.5$	V
$CMRR$	Common-mode rejection ratio	$V_S = \pm 15\text{ V}$, $V_{CM} = -10$ to $+10\text{ V}$		104		dB
		$V_{CM} = -15$ to 13.5 V , $T_A = -40$ to $+125^\circ\text{C}$	65	102		
OPEN-LOOP GAIN						
A_{VOL}	Open-loop voltage gain	$V_S = 15\text{ V}$, $V_O = 1$ to 10 V , $R_L \geq 2\text{ k}\Omega$ to V_-		110		dB
		$T_A = -40$ to $+125^\circ\text{C}$		105		
FREQUENCY RESPONSE						
GBW	Gain bandwidth product			1.3		MHz
SR	Slew rate	$V_S = 36\text{ V}$, $G = +1$, 10 V step		0.98		$\text{V}/\mu\text{s}$
THD+N	Total harmonic distortion + noise	$G = +1$, $f = 1\text{ kHz}$, $V_O = 3\text{ V}_{RMS}$		0.00398		%
OUTPUT						
V_{OH}	High output voltage swing	$V_S = \pm 18\text{ V}$, $R_L = 10\text{ k}\Omega$		$V_{S+} - 100$		mV
		$V_S = \pm 18\text{ V}$, $R_L = 2\text{ k}\Omega$		$V_{S+} - 270$		
V_{OL}	Low output voltage swing	$V_S = \pm 18\text{ V}$, $R_L = 10\text{ k}\Omega$		$V_{S-} + 60$		mV
		$V_S = \pm 18\text{ V}$, $R_L = 2\text{ k}\Omega$		$V_{S-} + 250$		
I_{SC}	Short-circuit current	$V_{S+} = +15\text{ V}$, $V_{S-} = -15\text{ V}$, $V_O = 0\text{ V}$		± 20	± 40	mA
POWER SUPPLY						
V_S	Operating Supply Voltage	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	3		36	V
I_Q	Quiescent current (per amplifier)	$V_S = 5\text{ V}$		300		μA
		$V_S = 36\text{ V}$		375	500	

Typical Characteristics

At $T_A = +25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, unless otherwise noted.

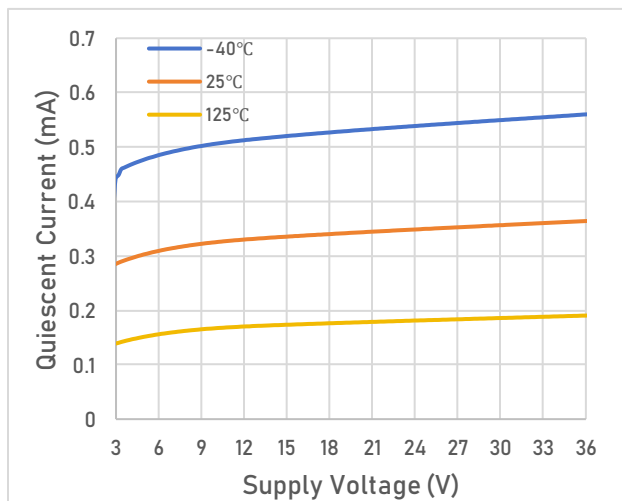


Figure 1. Quiescent Current vs Supply Voltage

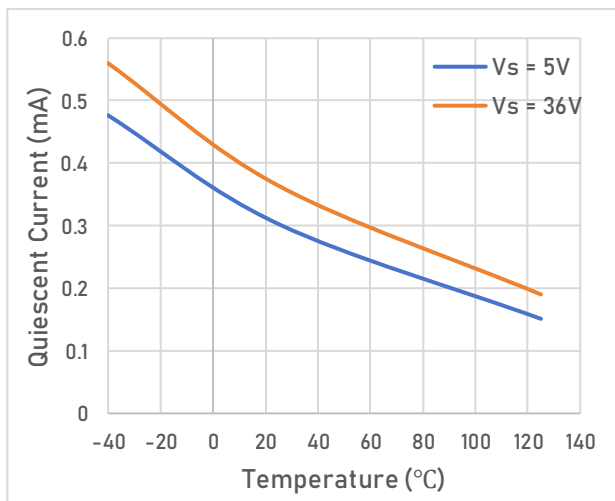


Figure 2. Quiescent Current vs Temperature

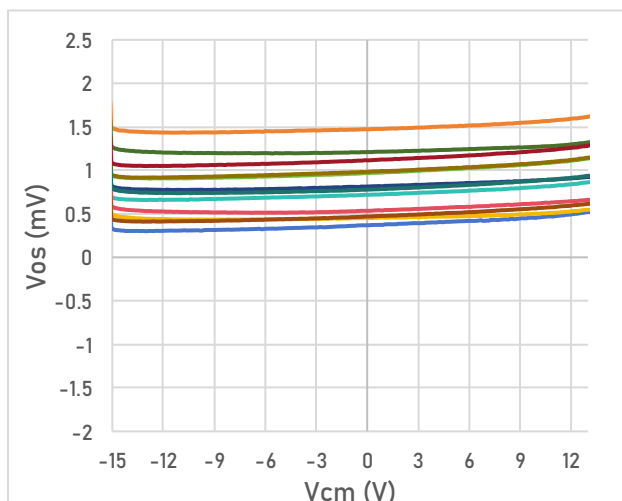


Figure 3. Offset voltage vs Common-mode Voltage

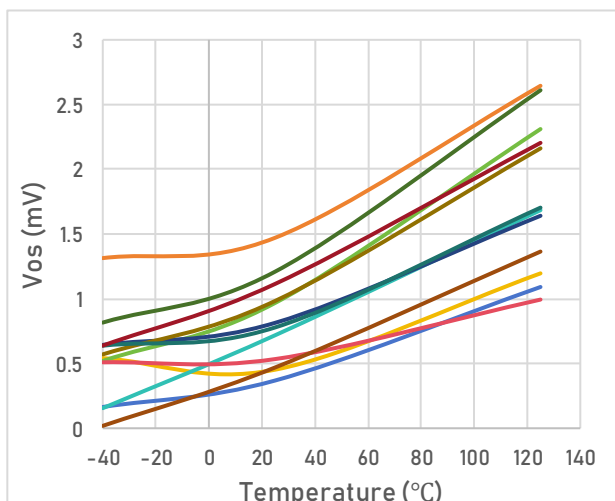


Figure 4. Offset voltage vs Temperature

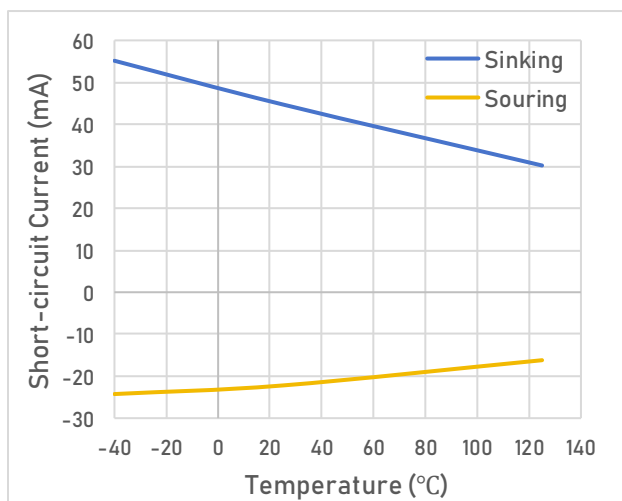
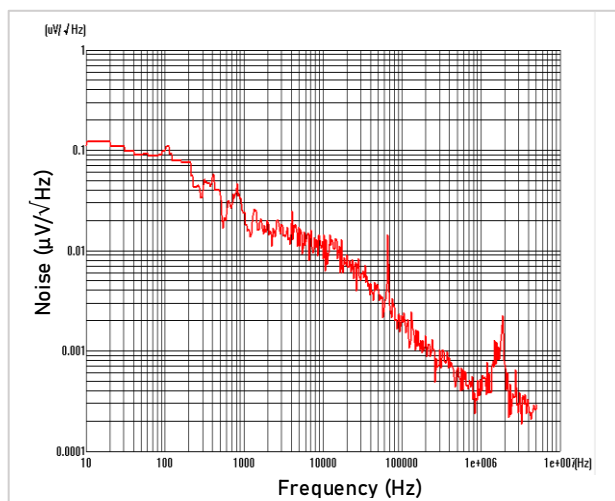
Figure 5. Short-circuit current vs Temperature $V_S=30\text{V}$ 

Figure 6. Input Voltage Noise Spectral Density vs Frequency

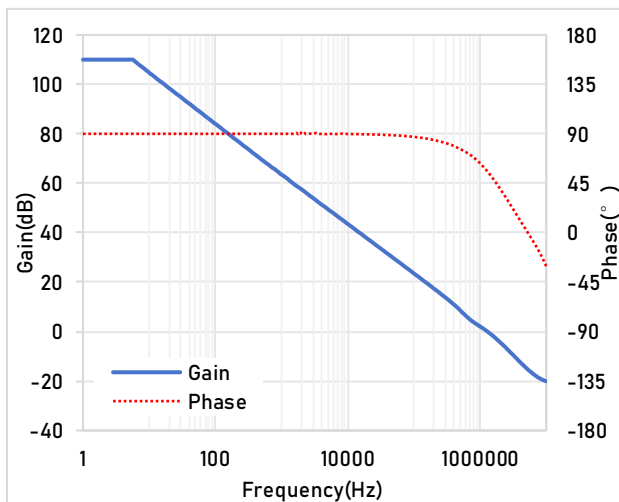


Figure 7. Open-Loop gain and phase vs Frequency

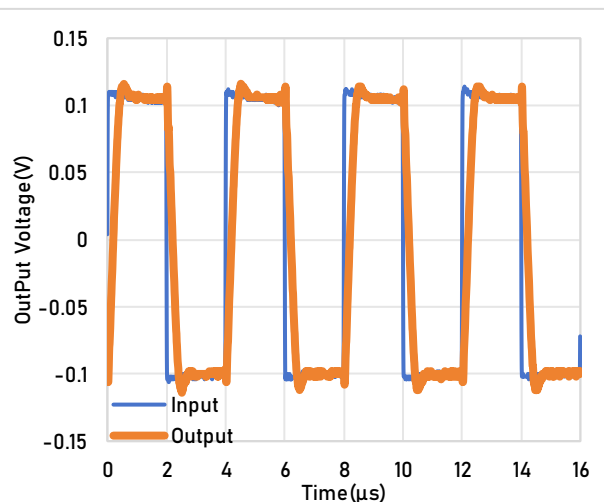


Figure 8. Small signal step response, G=1

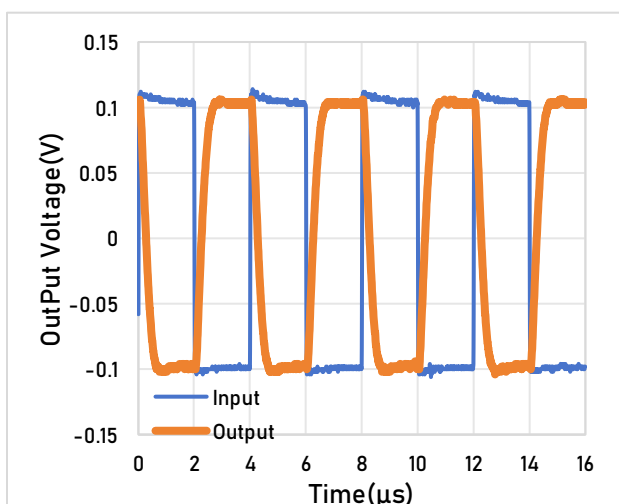


Figure 9. Small signal step response, G= -1

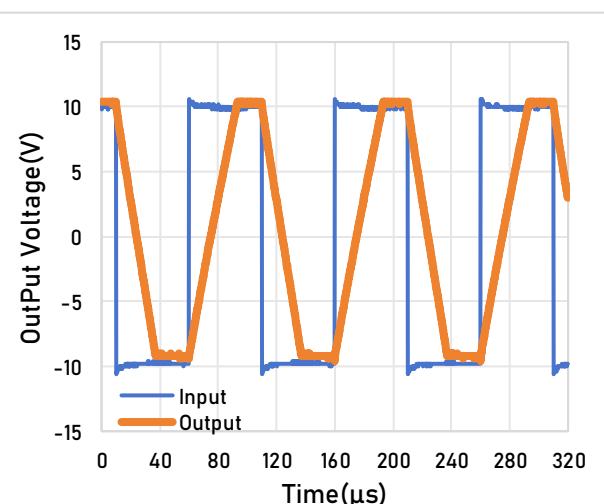


Figure 10. Large signal step response, G= 1

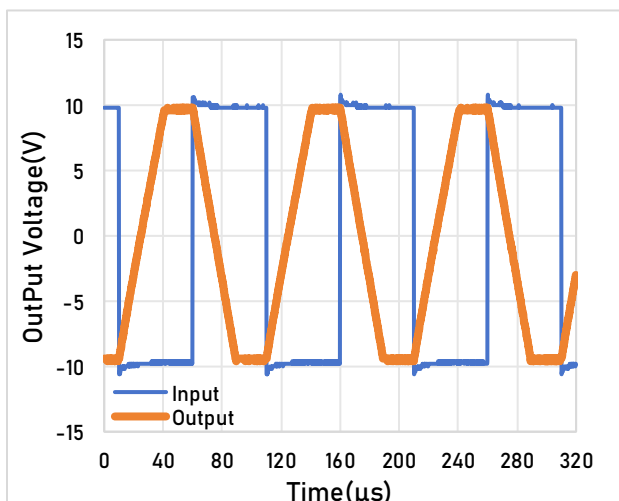


Figure 11. Large signal step response, G= -1

CAUTION: These devices are sensitive to electrostatic discharge. Follow proper IC Handling Procedures.
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Detailed Description

Operating Voltage

The LTA321 / LTA323 / LTA2904 / LTA2902 family of 36 V General-purpose low power amplifiers is fully specified and ensured for operation from 3 V to 36 V and offers an combination with quiescent supply current of 300 μ A per amplifier. In addition, and many specifications apply over the industrial temperature range of -40°C to $+125^{\circ}\text{C}$, parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

Maximizing performance through proper layout

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the LTA321 / LTA323 / LTA2904 / LTA2902 devices, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the comparator inputs further reduces leakage currents. Figure 6 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both input. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

Other potential sources of offset error are thermo-electric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

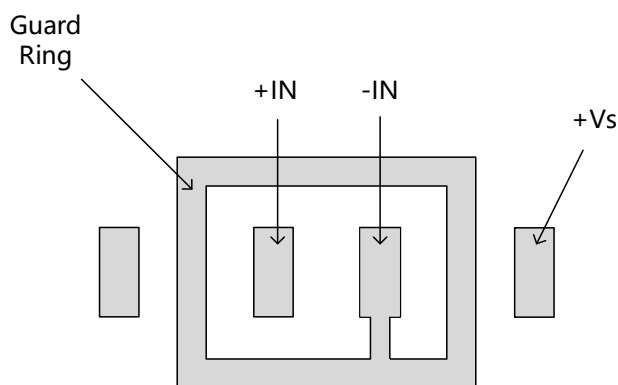


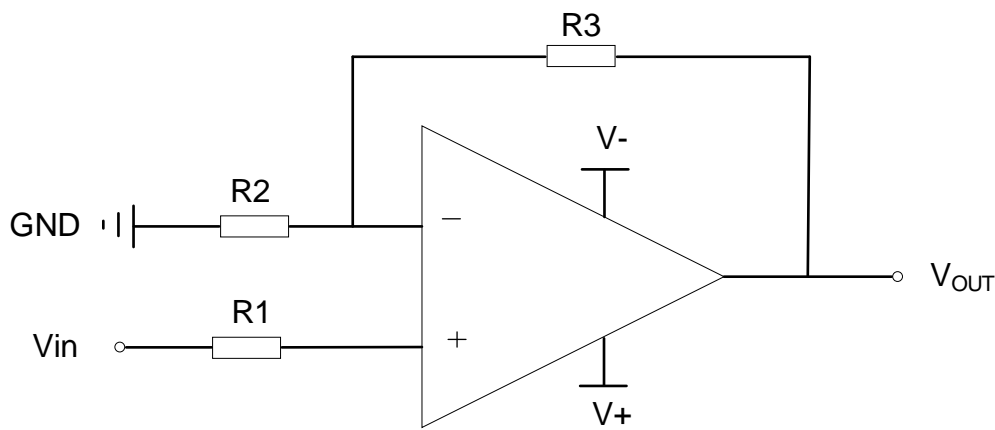
Figure 6: Use a guard ring around sensitive pins

Input and Output coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Typical Application Circuits

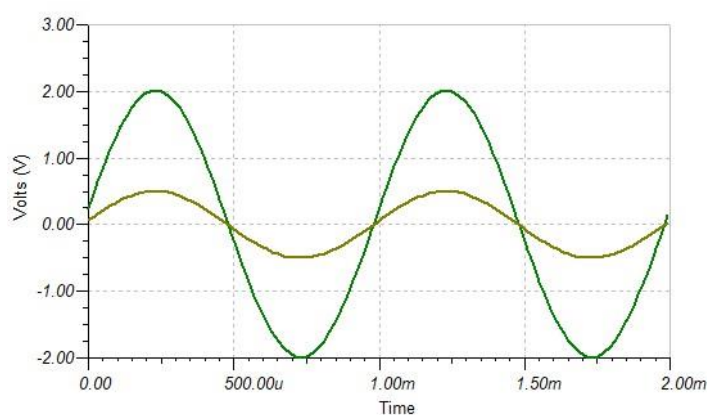
Non-Inverting Amplifier



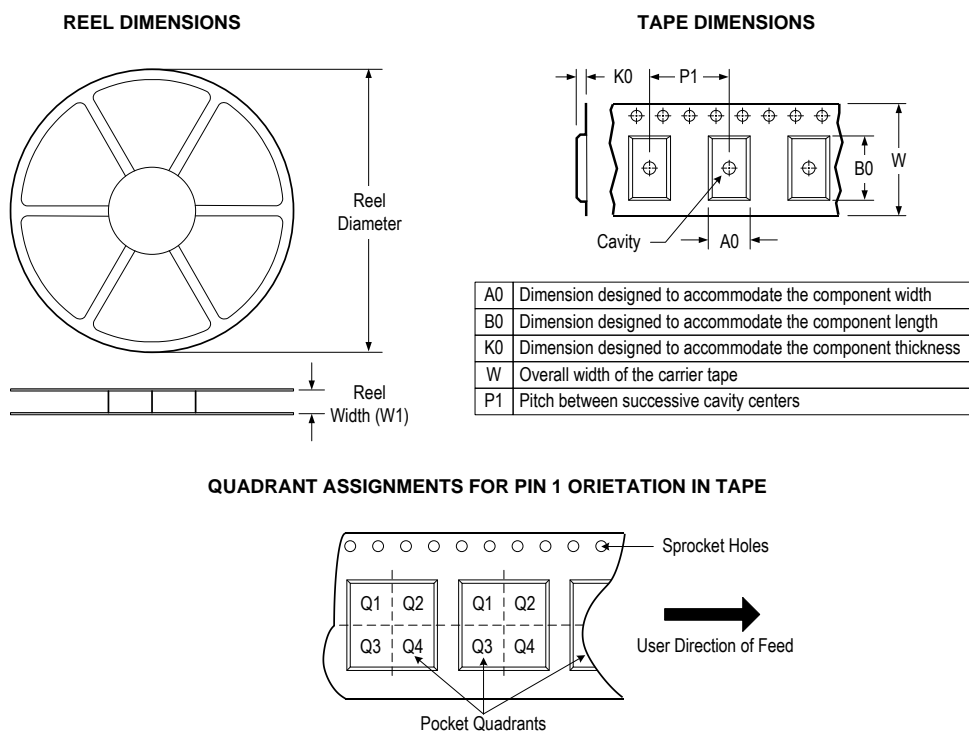
Non-inverting Amplifier is one of typical application for an Op-AMP. With V_{in} to $IN+$ and V_{OUT} will be amplified by Equation (1).

$$V_{OUT} = \left(1 + \frac{R3}{R2}\right) * V_{IN} \quad (1)$$

For example: If V_s is ± 12 V, V_{in} signal requires to scale from ± 0.5 V to ± 2 V. Consider to choose Resistors in kilohm range because the input current of amplifier is limited to milliampere range. $R1$, also known as balance resistance, is usually taken as the parallel resistance value of $R2$ and $R3$, used to eliminate bias current errors. In this example, we finally use $9\text{ k}\Omega$ for $R1$, $12\text{ k}\Omega$ for $R2$, $36\text{ k}\Omega$ for $R3$.



Tape and Reel Information

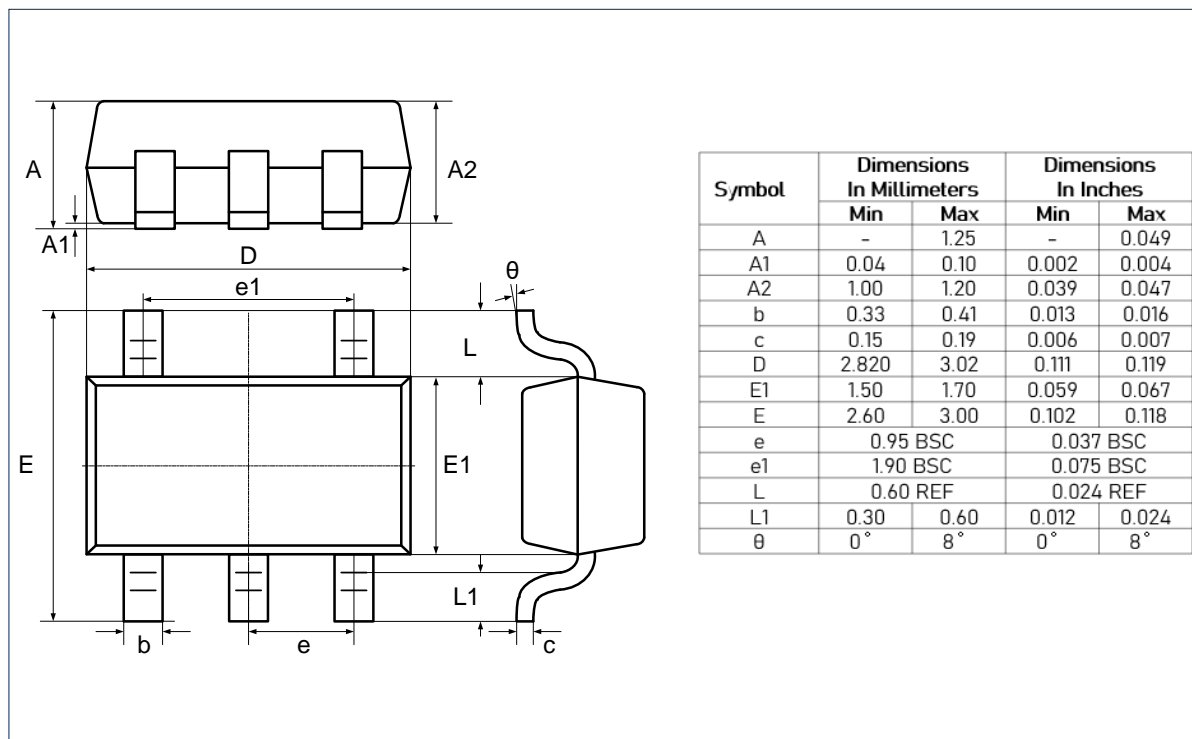


* All dimensions are nominal

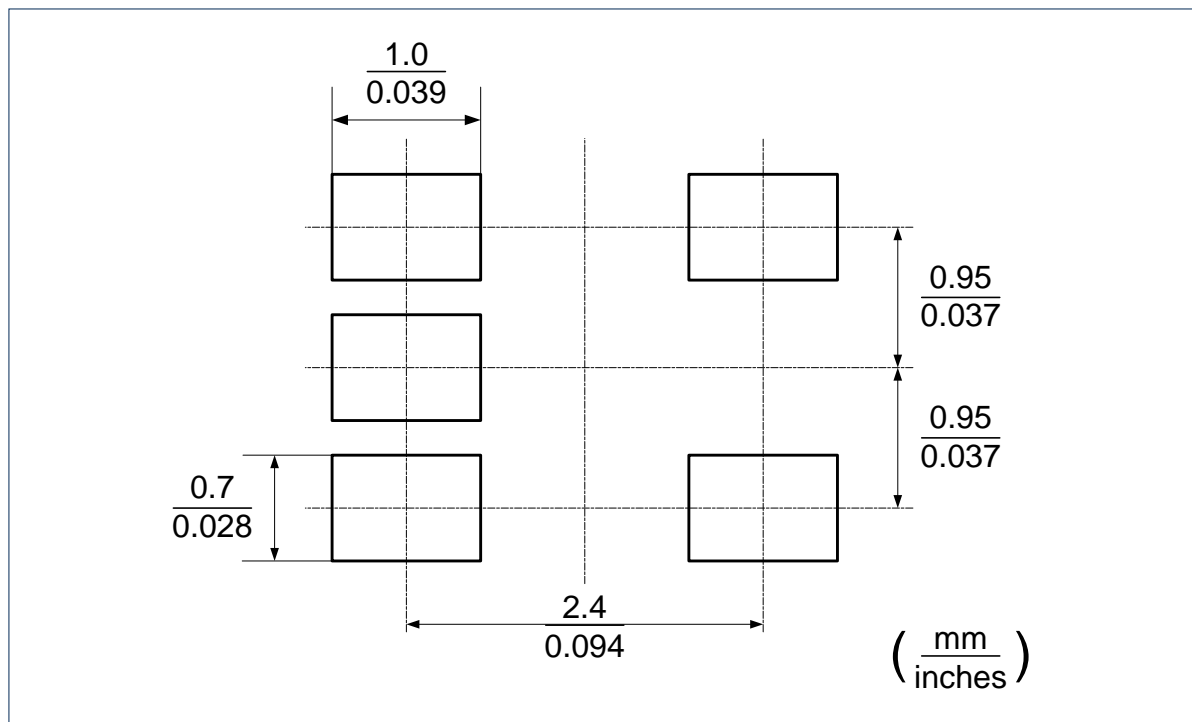
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA321JXT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA323JXT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA2904XS8/R8	SOIC	8	4 000	330	12.4	6.6	5.3	2.0	8.0	12.0	Q1
LTA2904XV8/R6	MSOP	8	3 000	330	12.4	5.0	3.5	2.0	8.0	12.0	Q1
LTA2904XT8/R6	TSSOP	8	3 000	330	16	8.5	7	2.0	8	1.2	Q1
LTA2902XS14/R5	SOIC	14	2 500	330	18	8.5	1.1	2.0	8.5	1.6	Q1
LTA2902XT14/R6	TSSOP	14	3 000	330	18	8.5	1.1	2.0	8.5	1.6	Q1

Package Outlines

DIMENSIONS, SOT23-5L

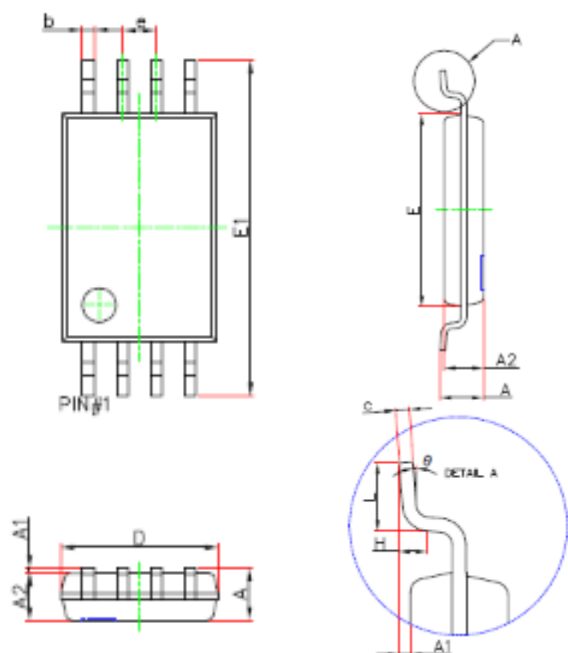


RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



Package Outlines (Continued)

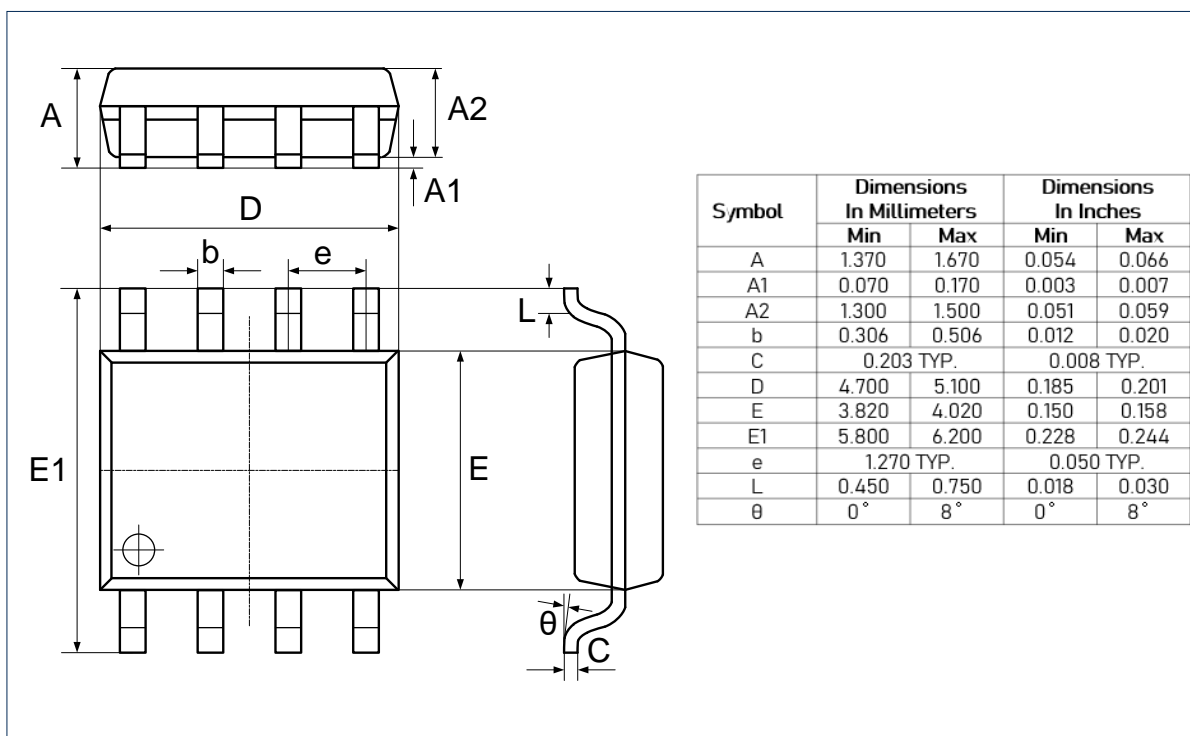
DIMENSIONS, TSSOP-8L



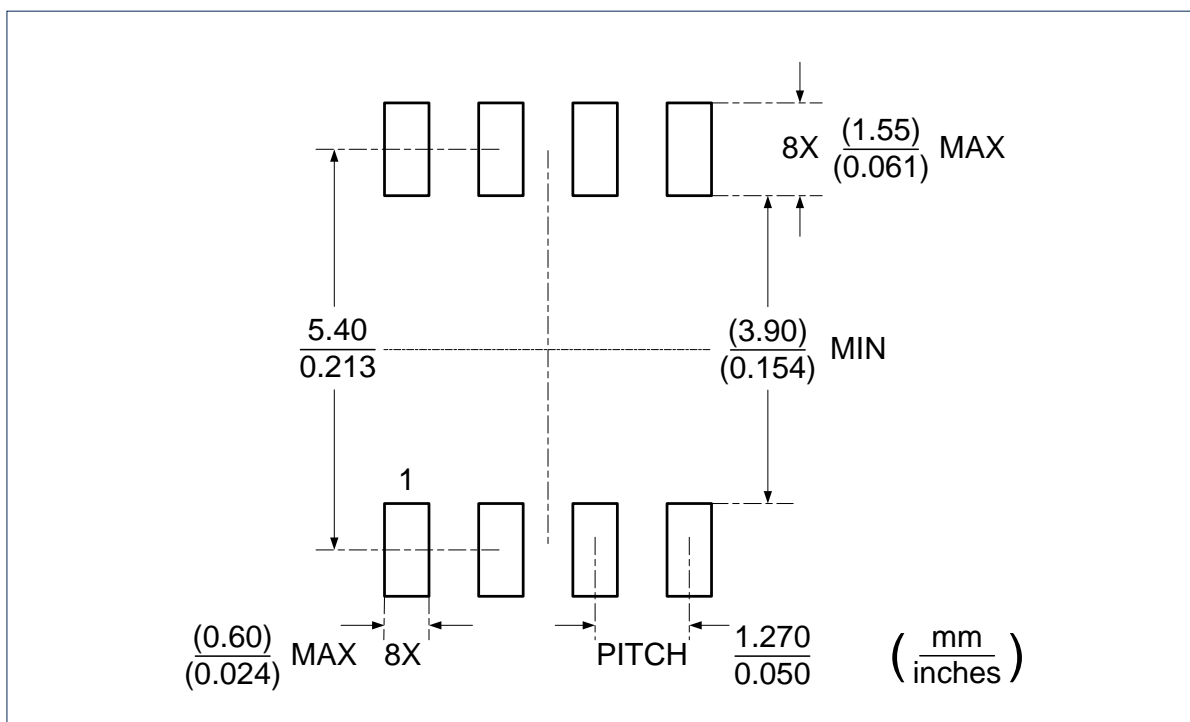
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	—	1.200	—	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	7°

Package Outlines (Continued)

DIMENSIONS, SOIC-8L

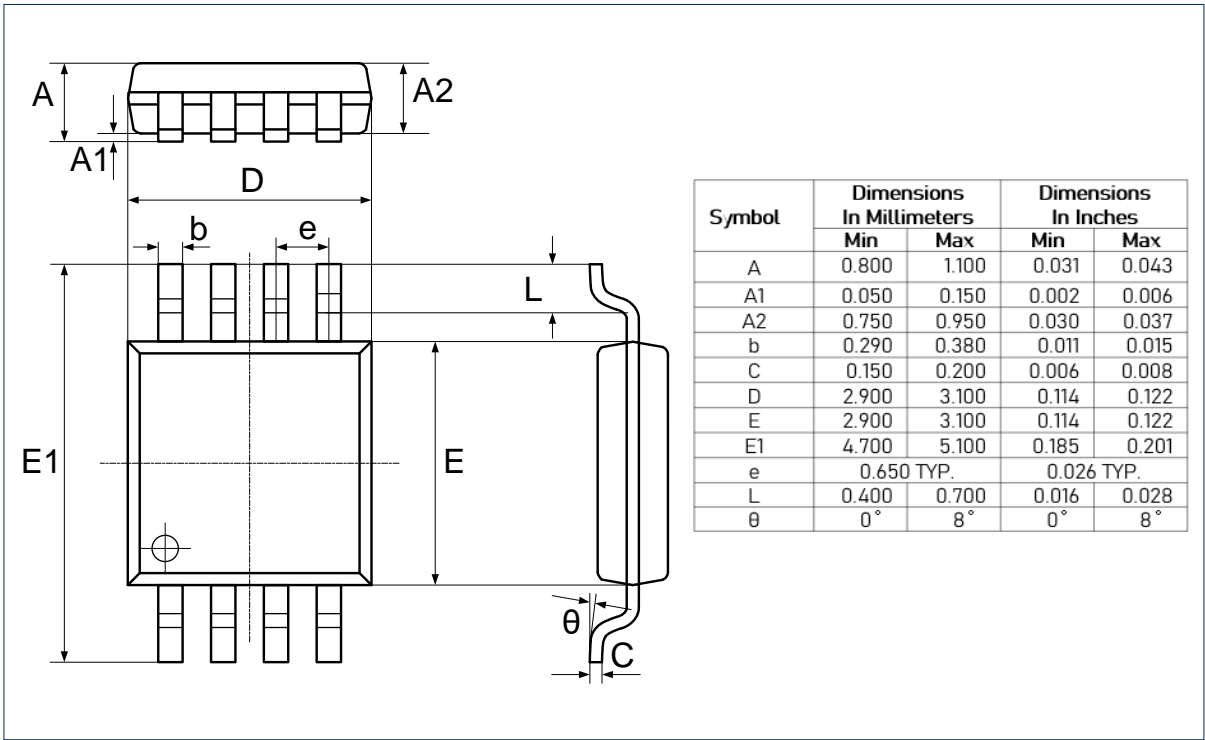


RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L

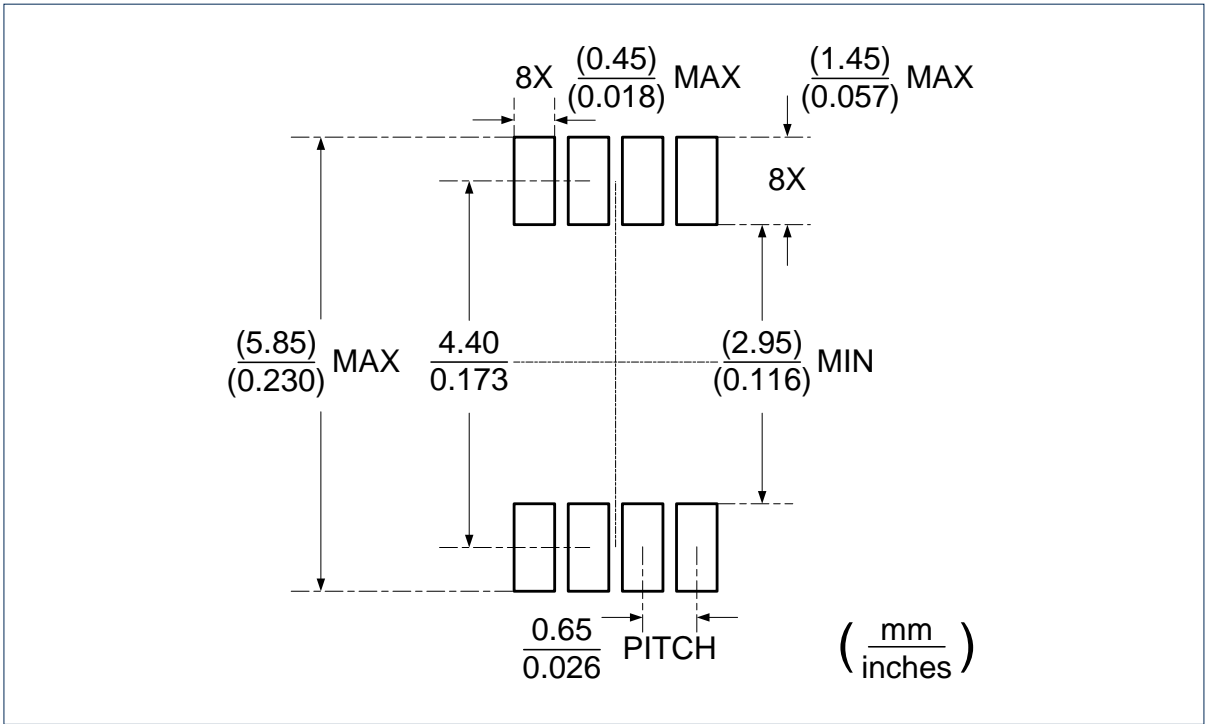


Package Outlines (Continued)

DIMENSIONS, MSOP-8L

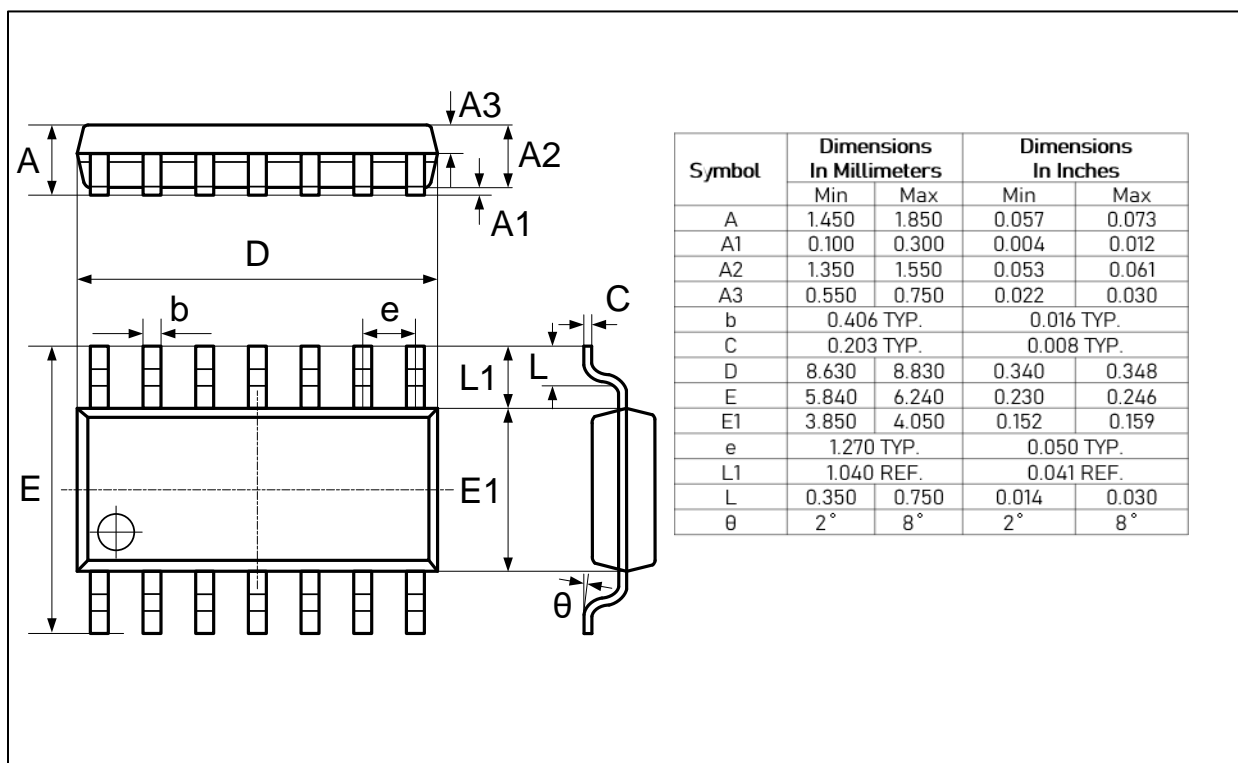


RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L

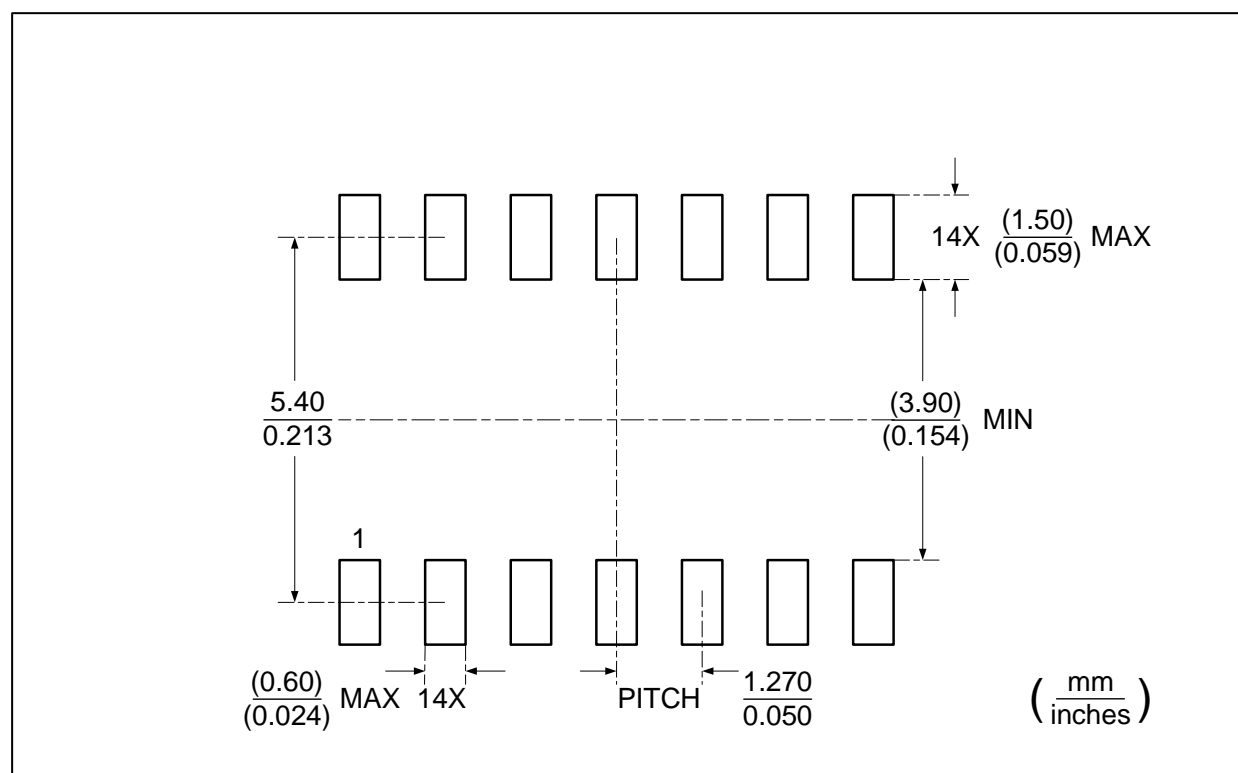


Package Outlines (Continued)

DIMENSIONS, SOIC-14L

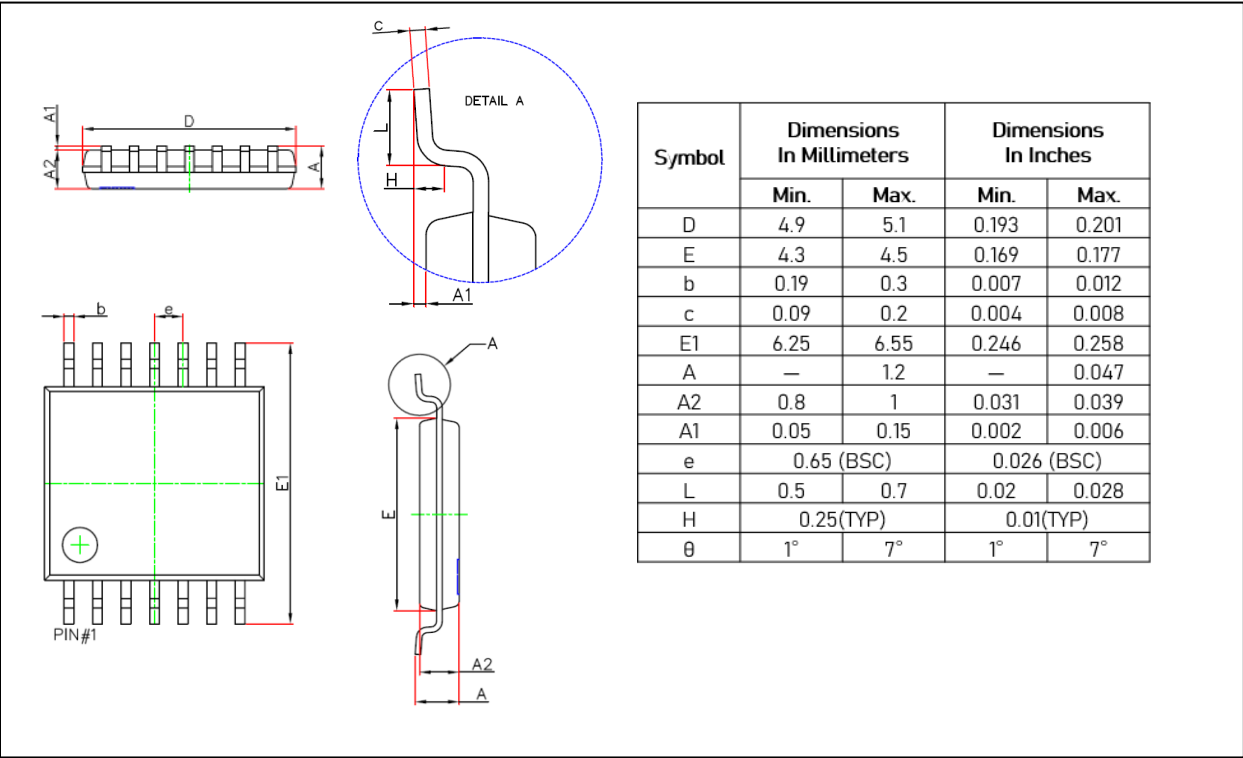


RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L

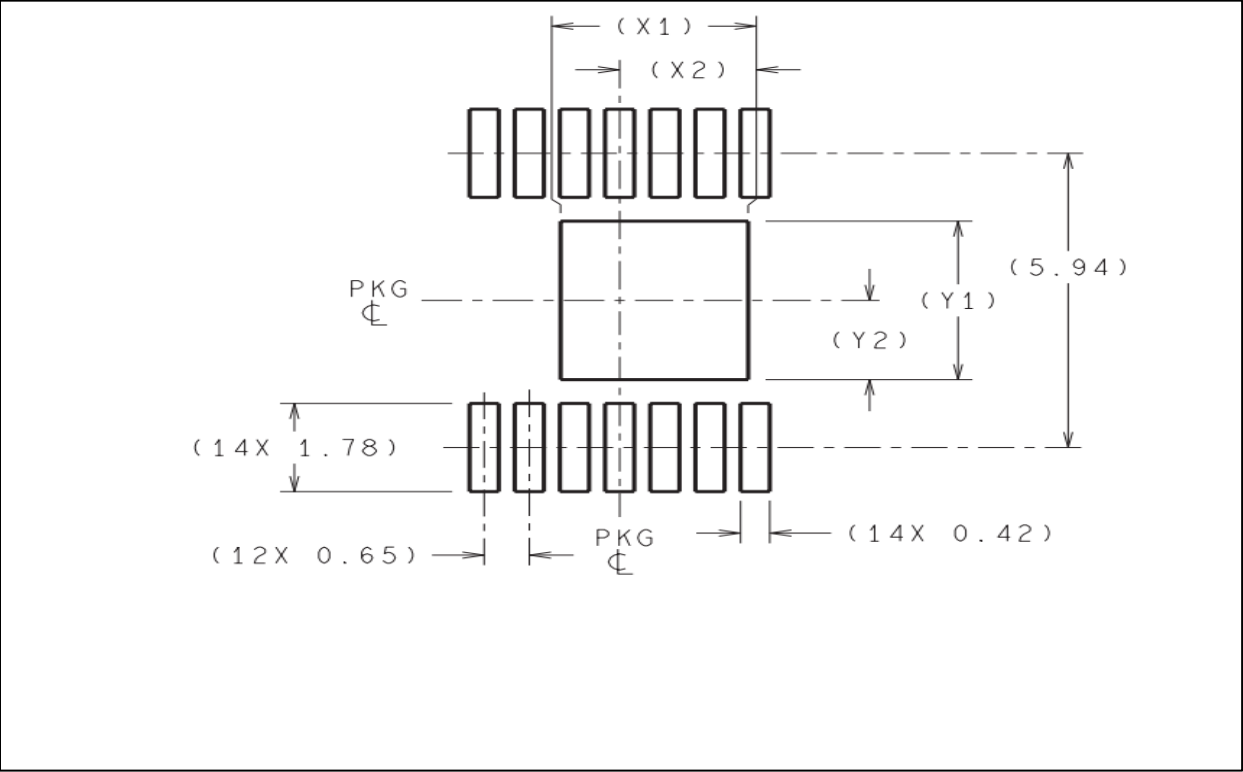


Package Outlines (Continued)

DIMENSIONS, TSSOP-14L

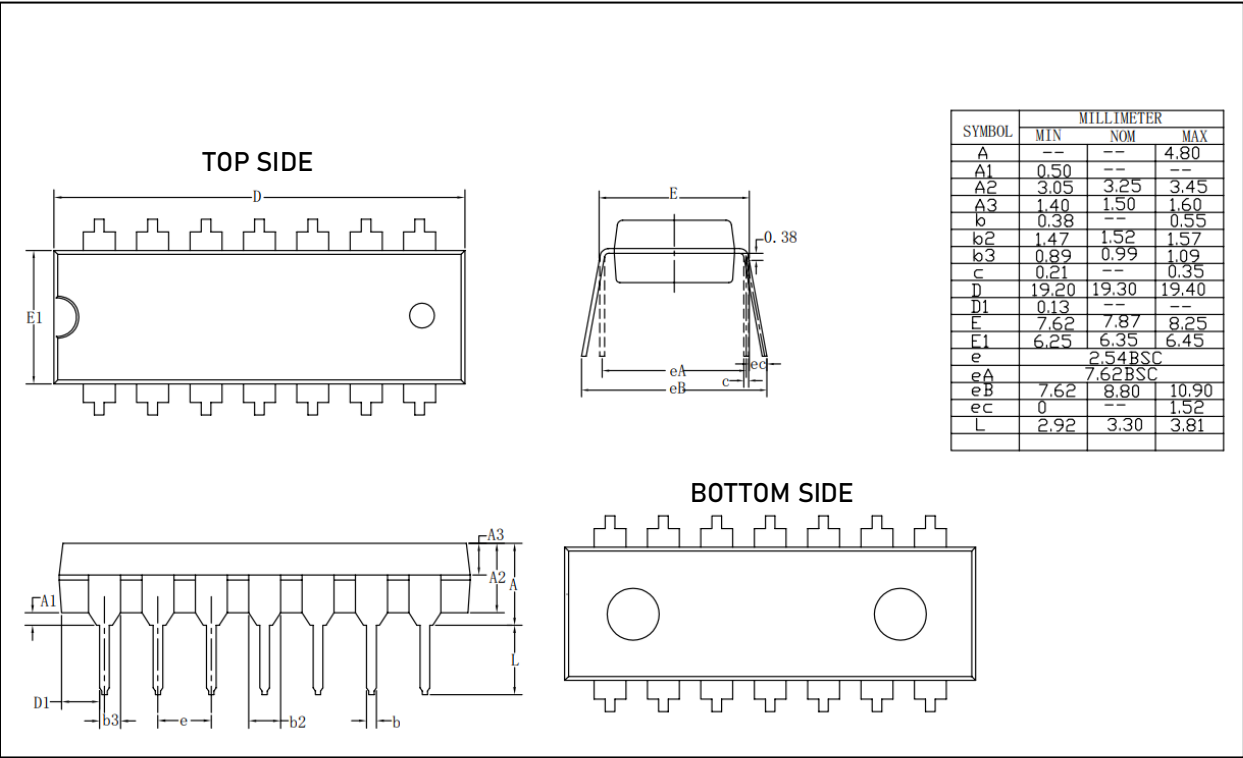


RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L

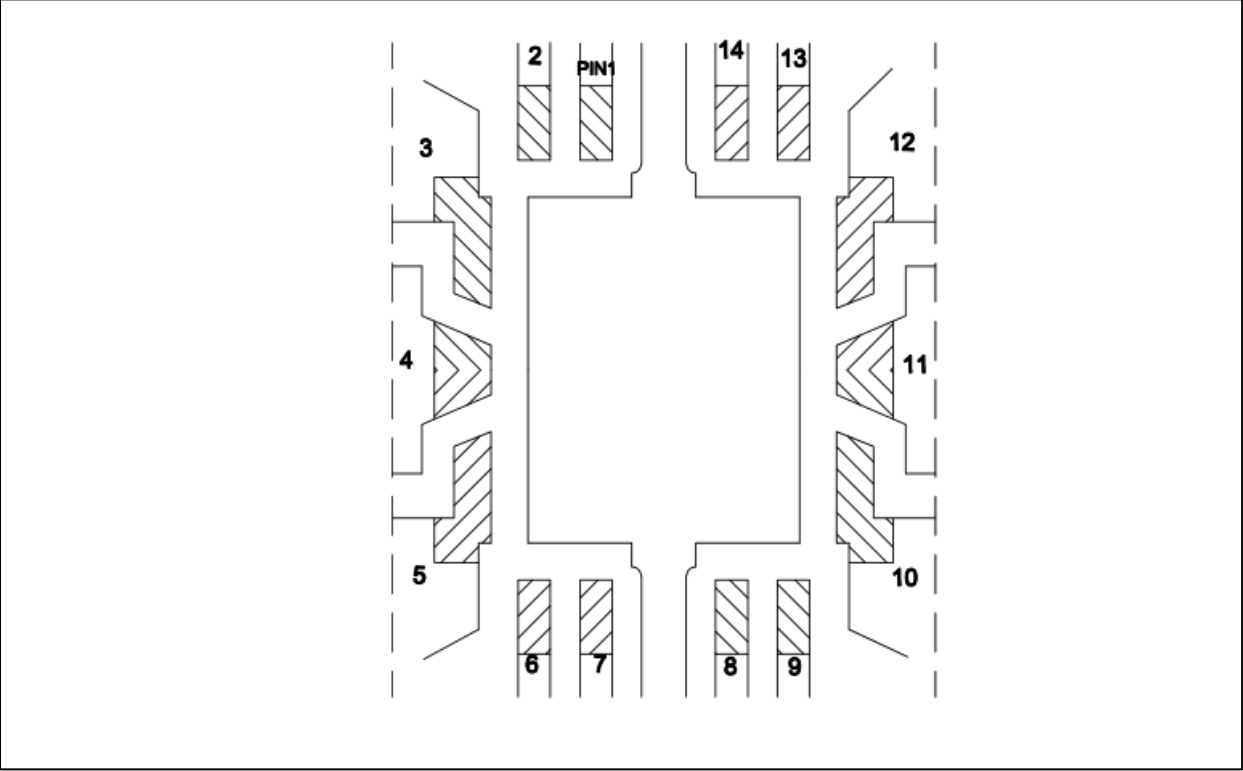


Package Outlines (Continued)

DIMENSIONS, DIP-14L



RECOMMENDED SOLDERING FOOTPRINT, DIP-14L



Important Notice

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