General Description

The LTP5070 is used for PWM speed control to drive DC motors, with an integrated H-bridge driver and control circuit, peak output current ±3.5 A, and a maximum operating voltage of 36 V. By inputting PWM control signals through the input ports IN1 and IN2, the speed and direction of DC motors can be controlled. The internal synchronous adjustment circuit of the IC can reduce the power consumption during the PWM control process.

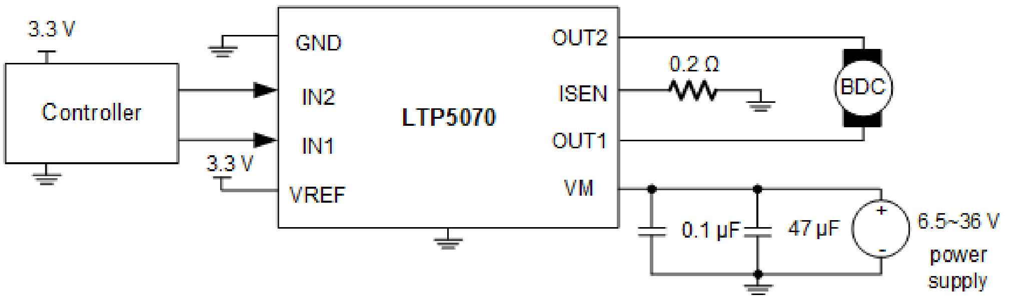
The LTP5070 device features integrated current regulation, based on the analog input VREF and the voltage on the ISEN pin, which is proportional to motor current through an external sense resistor.

The LTP5070 has an ultra-low power sleep mode. The IC has integrated over-current protection (OCP), motor lead to ground or power short circuit protection, Undervoltage Lockout (UVLO), and over-temperature protection (OTP).

The IC is packaged in an ESOP-8 package with exposed thermal pad to effectively dissipate heat from the chip.

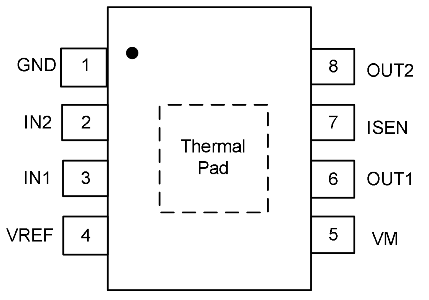
Features and Benefits

- Wide operating voltage range: 6.5 V to 36 V
- Low R$_{RDS(on)}$ (0.6 Ω @ 1 A)
- Low power standby mode
- Adjustable output current limit
- Integrated synchronized regulation
- Forward, reverse, brake and standby modes
- 3.5 A peak current drive
- Integrated protection features:
  - Undervoltage Lockout (UVLO)
  - Overcurrent protection (OCP)
    Motor short protection
    Motor lead short to ground protection
    Motor lead short to battery protection
  - Over-temperature protection (OTP)



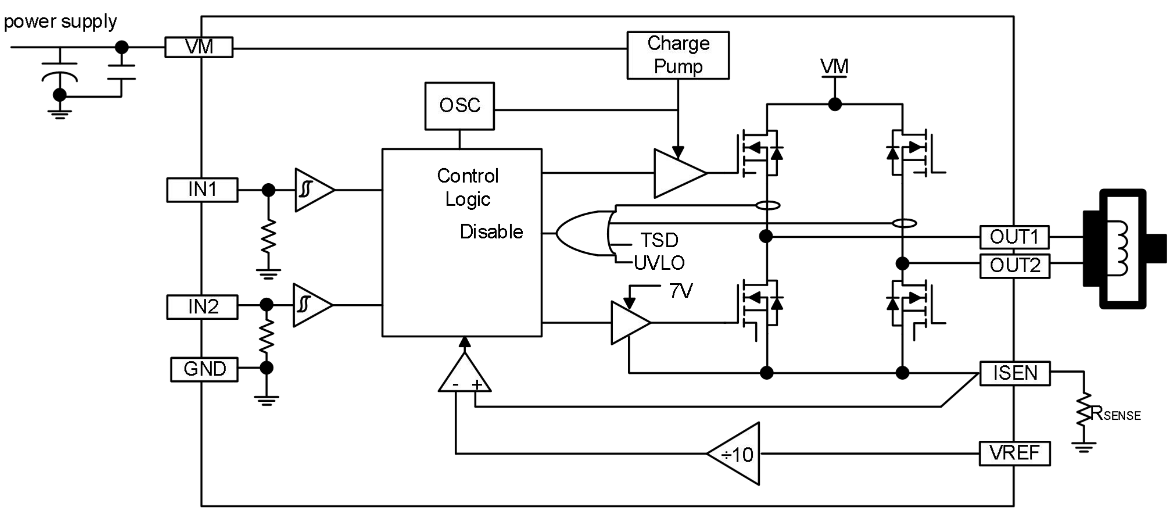
Pin Configurations (Top View)

ESOP-8



Pin no.	Symbol	Function
1	GND	Logic ground. Connect to board ground.
2	IN2	Input signal 2, internal pull-down resistor included.
3	IN1	Input signal 1, internal pull-down resistor included.
4	VREF	Analog input.
5	VM	Power supply, need to connect the input electrolytic capacitor to avoid instantaneous spikes.
6	OUT1	H - Bridge Output 1, connected to OUT2 via the load.
7	ISEN	Adjust the drive current limit pin to set the current limit threshold by connecting a power resistor to ground, if no current limit adjustment is required the ISEN pin can be connected directly to ground.
8	OUT2	H - Bridge Output 2, connected to OUT1 via the load.
/	Thermal pad	Heat sink, needs to be connected to ground.

Block Diagram



Ordering Information[1]

Ordering Number[Note1]	Package	Operating Temperature	Packing Option	Silk Printing
LTP5070K/R8	ESOP8	−40 ℃ to 125 ℃	Tape and Reel, 4 000	5070K

(1) Please contact your Linearin representative for the latest availability information and product details.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Value	Unit
Power Supply Voltage	V_M		40	V
Logic Input Voltage (IN1, IN2)	V_{IN}		-0.3 to 6	V
Vref input voltage	V_{REF}		-0.3 to 6	V
Current sense input pin voltage (ISEN)	V_S		-0.5 to 0.5	V
OUT1,2 output voltage	V_{OUT}		-2 to V_M+2	V
Output Current	I_{OUT}	PWM duty cycle 100%	3.5	A
Peak output current	I_{out}	t_W < 500 ns	6	A
Operating Temperature Range	T_A	Temperature Range K	-40 to 125	°C
Maximum Junction Temperature	$T_{J(MAX)}$		150	°C
Storage temperature	T_{STG}		-55 to 150	°C

Note: Stresses exceeding those listed in the Maximum Rating table may damage the device. Operation beyond the maximum Rating conditions or under harsh conditions may affect product reliability and function.

ESD Ratings

Parameter		Value	Unit
V(ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	8000	V
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002	1000	V

Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY(VM)						
VM Operating voltage	VM		6.5		36	V
VM Operating current	I_{VM}	VM = 12 V		3	10	mA
VM sleep current	$I_{VMSLEEP}$	VM = 12 V			10	μA
Turn-on time	ton	VM > V_{UVLO} with IN1 or IN2 high		40	50	μs
Logic input parameters						
Input logic low voltage	V_{IL}				0.5	V
Input logic high voltage	V_{IH}		1.5			V
Input logic hysteresis	V_{HYS}			0.5		V
Input logic low current	I_{IL}	VIN = 0 V	-1		1	μA
Input logic high current	I_{IH}	VIN = 3.3 V		33	100	μA
Pulldown resistance	$R_{(PD)}$	to GND		100		kΩ
Propagation delay	$t_{(PD)}$	INx to OUTx change		0.7	1	μs
Time to sleep	t_{sleep}	Inputs low to sleep		1	1.5	ms
MOTOR DRIVER OUTPUTS(OUT1, OUT2)						
High-side FET on res	$R_{DS(ON)}$	VM=24 V，I=1A		316	400	mΩ
Low-side FET on res	$R_{DS(ON)}$	VM=24 V，I=1A		258	300	mΩ
Output dead time	t_{DEAD}			220		ns
Body diode forward voltage	Vd	I_{OUT}=1A		0.8	1	V
CURRENT REGULATION						
ISEN gain	A_V		9.4	10	10.4	V/V
PWM off-time	t_{OFF}			25		μs
PWM blanking time	t_{BLANK}			2		μs
Protection circuit parameters						
VM Undervoltage Lockout	V_{UVLO}	VM decreasing		6.1	6.4	V
		VM increasing		6.3	6.5	V
VM Undervoltage Lockout hysteresis	$V_{UVLOhys}$		100	180		mV
Overcurrent protection trip	I_{OCP}		3.6	4.5	6.4	A
Overcurrent deglitch time	t_{OCP}			1.5		μs
Overcurrent retry time	t_{RETRY}			3		ms
Thermal shutdown temperature	T_{SD}	Temperature increasing	165	180		℃
Thermal shutdown hysteresis	T_{SDhys}			40		℃

Notes: TJ =25℃, VM =24V, OUT terminal connect 1nF capacitor to ground respectively, special conditions are described separately.

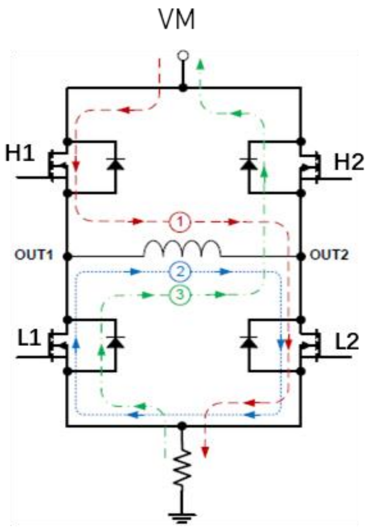
Typical Performance Characteristics

Current path

① IN1=1, IN2=0; H1,L2 on; H2,L1 off.

② IN1=1, IN2=1; H1,H2 off; L1, L2 on, keep t_{off} or L1, L2 off after current decay to 0.

③ IN1=0, IN2=0; H1,L2 off; H2,L1 on, maintain t_{off} or current decay to 0 after H2,L1 off.

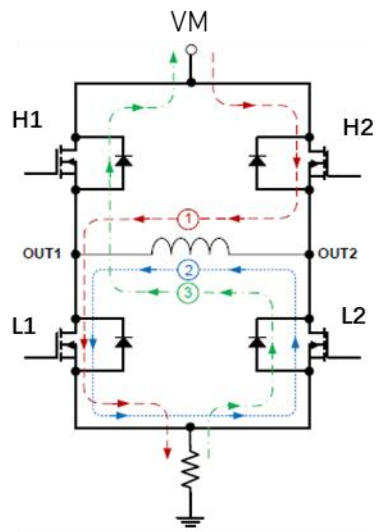


Forward

① IN1=0, IN2=1; H2,L1 on; H1,L2 off

② IN1=1, IN2=1; H1,H2 off; L1, L2 on, keep t_{off} or L1, L2 off after current decay to 0.

③ IN1=0, IN2=0; H1,L2 off; H2,L1 on, maintain t_{off} or current decay to 0 after H2,L1 off.



Revers

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM)for variable motor speed. When using PWM, it typically works best to switch between driving and braking. For example, to drive a motor forward with 50% of its max RPM, IN1 = 1 and IN2 = 0 during the driving period, andIN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current decay is also available. The input pins can be powered before VM is applied.

Control Truth Table

IN1	IN2	OUT1	OUT2	Functionality
0	0	Z	Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake;low-side slow decay

Note: Z indicates high impedance.

LINEARIN

Functional Description

Overview

The LTP5070 is designed to operate brushed DC motors. The output driver H-bridges, consist of low resistance N-channel D-MOSFET with internal synchronization regulation to reduce the power consumption. The H-Bridge output current is regulated by a pulse-width modulation (PWM) with a fixed off-time. the IN1 and IN2 inputs control the bridge separately.

Protection includes thermal shutdown (OTP), Overcurrent protection (OCP), Undervoltage lockout protection (UVLO) prevents damage by holding the output off until the drive reaches sufficient operating voltage.

Low power standby mode

The device enters the low-power standby mode when both input (INx) pins are low for more than 1 ms. The low-power standby mode shuts down most of the internal circuitry, including the charge pump and voltage regulator. When the LTP5070 exits standby mode, it needs to wait for the charge pump to ramp up to a stable voltage (with a maximum delay of 1.5 µs) before it can receive PWM commands.

Internal PWM current control

The IC turns on the diagonal upper and lower FET outputs first, and the current passes through the motor windings and the optional external current sense resistor RS . When the voltage drop across RS exceeds the threshold set by the comparator, the PWM control is suspended, and the lower and upper FETs are turned off automatically (in mixed decay mode).

V_{REF}

Setting the maximum current limit $I_{TripMAX}$ (A). via external R_S and V_{REF}.

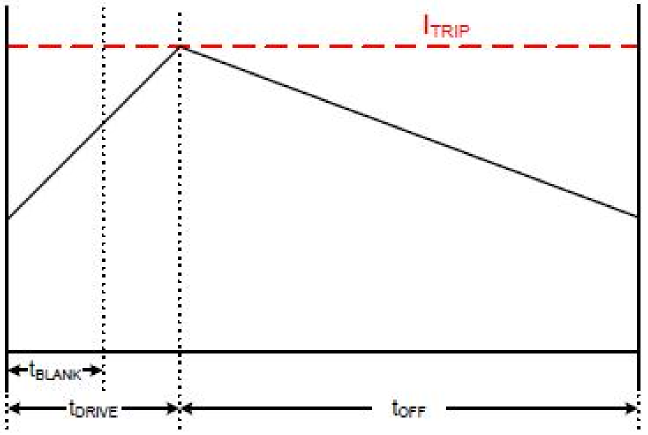
$$I_{TripMAX} = \frac{V_{REF}}{10 \times R_S}$$

Where VREF is the input voltage on the VREF pin, RS is the resistance (Ω) of the sense resistor on the ISEN pin.

For example, if VREF = 3.3 V and a RISEN = 0.15 Ω, the DRV8870 will limit motor current to 2.2 A no matter how much load torque is applied.

When ITRIP has been reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for time tOFF (typically 25 µs).

After tOFF has elapsed, the output is re-enabled according to the two inputs INx. The drive time (tDRIVE) until another ITRIP event heavily depends on the VM voltage, the motor's back-EMF, and the motor's inductance.



Overcurrent protection (OCP)

An internal current monitoring circuit protects the IC from damage due to an output short circuit. When a short circuit is detected, the IC will latch the fault and disable the output. Fault lockout can only be cleared by exiting low power standby mode or by restarting VM power up. During overcurrent protection, limit operating parameters may be exceeded for a short period of time before the IC locks out.

Automatic switching off

If the IC (DIE) temperature rises to approximately 165℃, the H-Bridge outputs will be switched off until the internal temperature drops by more than 40℃ (hysteresis parameter TSDhys). An internal undervoltage protection circuit （UVLO） detects the voltage on VM to prevent switching on the output driver if VM falls below the UVLO threshold.

Braking

IN1 and IN2 input logic are high level at the same time, the IC enters the braking state, OUT1 and OUT2 both output low level, the motor winding current into the slow decay mode. Or after detecting that the output exceeds the limit current, the bridge enables the chop action, the IC will also temporarily enter the braking state (see PWM control truth table). Because the current can be driven in both directions by the DMOS switches, this path setting effectively reduces the BEMF generated by the motor when enabling the Chop action. The maximum current in the path can be approximated as VBEMF / RL . It is important to note that in the worst braking case (high speed, high inertia loads) this current does not exceed the chip's limiting operating parameters.

Synchronization

When the PWM off cycle is triggered by an internal fixed time off cycle (Toff), the load current will remain circulating. The synchronous regulation turns on the D-MOSFETs on the current path during the current decay, bypassing their body diodes with DMOSFETs with low on-resistance RDS(on). This greatly reduces the IC power consumption. When a current decay of 0 is detected, the synchronous regulation is turned off to prevent load current reversal.

APPLICATION INFORMATION

Current Sampling Pin (ISEN)

To use PWM motor control, place a low resistance resistor RS between the ISEN pin and ground for current sampling. In order to minimize the effect of the resistive voltage drop of the ground resistor on the current sampling of RS , RS should have a separate connection to the star ground point as shown in Figure 4, which needs to be as short as possible because the PCB ground resistance has a large effect on the low-resistance resistor and must be taken into account.

The voltage can be sampled directly at both ends of Rs. It is not recommended to add a sense resistor to the GND pin. when selecting the resistance value of the resistor, make sure that the voltage at the ISEN pin does not exceed the maximum voltage ±500 mV at the maximum load. During the overcurrent protection occurs, it is possible that this maximum voltage may be exceeded for a short period of time.

Ground

The star ground point should be as close as possible to the LTP5070. The ground below the exposed thermal pad of the IC is a good location for the star ground point.

PCB Layout

The PCB should have a thick ground plane. For optimum electrical and thermal performance, the LTP5070 must be soldered directly to the PCB. At the bottom of the LTP5070 package is an exposed thermal pad that provides a path for enhanced heat dissipation. The thermal pad must be soldered directly to an exposed copper plane on the PCB for optimal heat transfer. Thermal vias are used to transfer heat to other layers of the PCB. It is recommended to increase the area of the top and bottom layers of the PCB to improve heat dissipation performance; keep the copper planes from the thermal pad to the rest of the board continuous; If these planes are interrupted, the thermal resistance will increase.

Input capacitor C2 affects the instantaneous load capacity, to avoid spikes, The recommended value of 100uF/50V or more, Cl and C2 need to be placed close to the VM pins; recommended PCB thermal pads using a diameter of 20mil, the hole size of 8mil heat dissipation holes, reduce thermal resistance. High-current paths (OUT1, OUT2, ISEN, VM etc.) as much as possible to increase the line width.

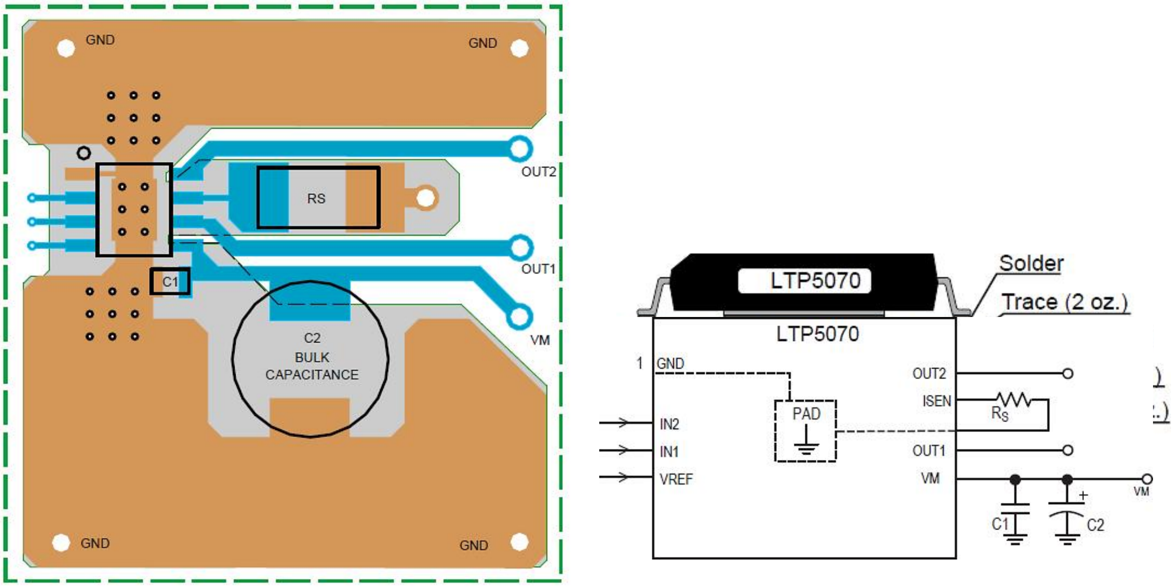


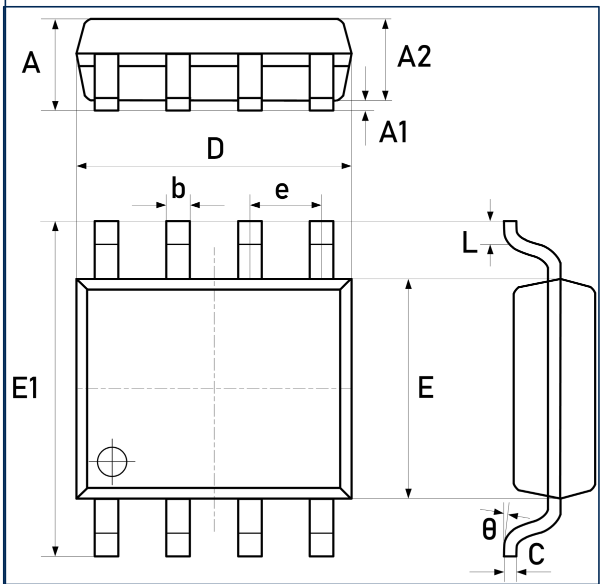
Figure 4. PCB Layout

Bill of Materials

SN	Name	Specification	Descriptions	Unit
1	R_S	0.25 (for VREF = 5 V, IOUT = 2 A)	2512, 1 W, 1% or better, carbon film chip resistor	Ω
2	C1	0.22	X5R minimum, 50 V or greater	µF
3	C2	100	Electrolytic, 50 V or greater	µF

Package Outlines

DEMENSIONS,SOIC-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.054	0.066
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.051	0.059
b	0.306	0.506	0.012	0.020
C	0.203 TYP.		0.008 TYP.	
D	4.700	5.100	0.185	0.201
E	3.820	4.020	0.150	0.158
E1	5.800	6.200	0.228	0.244
e	1.270 TYP.		0.050 TYP.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L