

General Description

The LTA37 provides the same high performance, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to $17V/\mu s$ and gain-bandwidth product to 82 MHz. The LTA37 provides the low offset and drift of the OP27 plus higher speed and lower noise. Offsets down to $50\mu V$ and a maximum drift of $0.5\mu V/^\circ C$ make the LTA37 ideal for precision instrumentation applications. Exceptionally low noise ($e_n=3nV/\sqrt{Hz}$ @1kHz), a low 1/f noise corner frequency of 5 Hz, and the high gain of 5.6 million, allow accurate high-gain amplification of low-level signals. The low input bias current of 50nA and offset current of 40nA are achieved by using a bias-current cancellation circuit.

The output stage has good load driving capability. A guaranteed swing of 10 V into 600Ω and low output distortion make the LTA37 an excellent choice for professional audio applications. PSRR 130 dB and CMRR 135 dB allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the LTA37 is achieved by using trimming circuit. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history. The LTA37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tape-head, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

LTA37 (single) is available in both SOIC-8L, MSOP-8L and TSSOP-8L packages. The LTA237 (dual) is offered in SOIC-8L and SOIC-16L packages.

Features and Benefits

- Low Noise, $0.2 \mu V_{p-p}$ (0.1 Hz to 10 Hz)
- $3nV/\sqrt{Hz}$ @1kHz
- Low Drift, $0.5\mu V/^\circ C$
- High Speed, $17 V/\mu s$ Slew Rate
- 82 MHz Gain Bandwidth
- Low Input Offset Voltage, $50\mu V$
- Excellent CMRR, 135 dB (Common-Voltage @ $\pm 11 V$)
- High Open-Loop Gain, 5.6 Million (135 dB)
- Nulling pin for further adjustment of V_{os} (Only for LTA37J series)
- Replaces OP27, OP37, OPA227, OPA228 SE5534, OP-200 In Gains > 5

Applications

- Precision Instrumentation
- Test Equipment
- Data Acquisition
- Professional Audio Equipment
- Motor Phase Current Sense
- Transducer Amplifier

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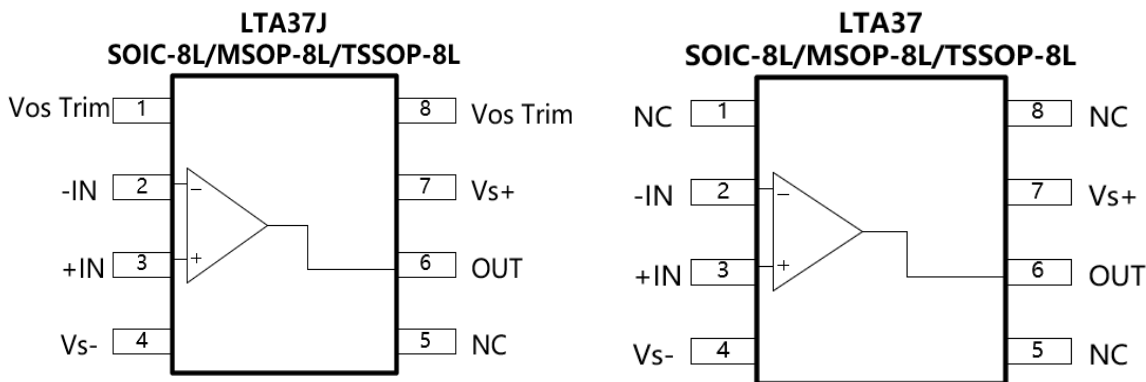
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Precision, Low Noise, High Speed Operational Amplifier ($A_{VCL} \geq 5$)

Ordering Information

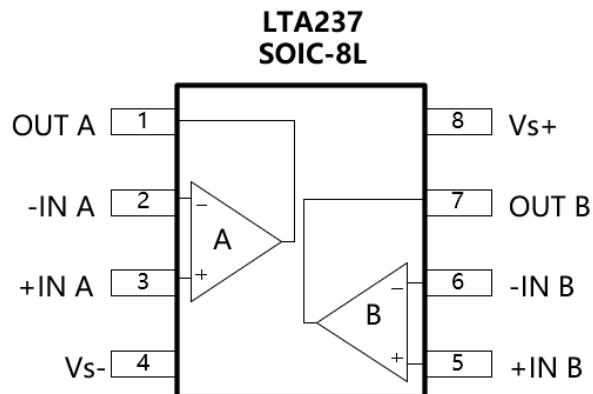
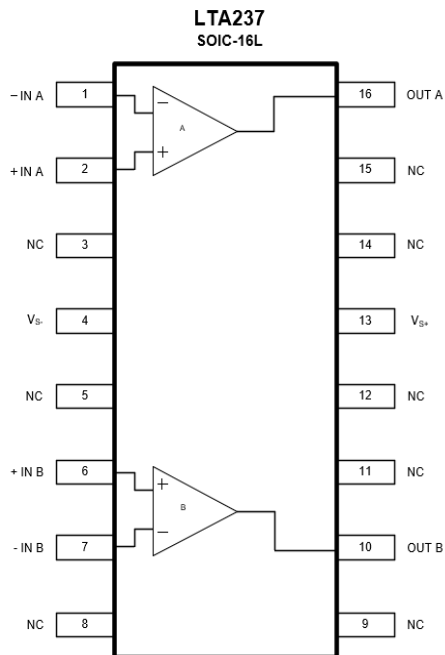
Part Number	Package Type	Package Size	Package Quantity	ECO Class	Mark Code
LTA37XS8/R8	SOIC-8L	4.90 mm * 3.92 mm	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	HJ37
LTA37XT8/R8	TSSOP-8L	4.40 mm * 3.00 mm	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	HJ37
LTA37XV8/R6	MSOP-8L	3.00 mm * 3.00 mm	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	HJ37
LTA37JXS8/R8	SOIC-8L	4.90 mm * 3.92 mm	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	H37J
LTA37JXT8/R8	TSSOP-8L	4.40 mm * 3.00 mm	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	H37J
LTA37JXV8/R6	MSOP-8L	3.00 mm * 3.00 mm	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	H37J
LTA237XS8/R8	SOIC-8L	4.90 mm * 3.92 mm	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	HJ237
LTA237XS16/R5	SOIC-16L	10.4 mm * 7.60 mm	Tape and Reel, 2 500	Green (RoHS & no Sb/Br)	HJ237

Pin Configuration (Top View)



PIN Name	SOIC-8L, MSOP-8L, TSSOP-8L	Description
V _{os} Trim / NC	1, 8	Nulling pin (only for J version). No Connection for Non-J Version.
-IN	2	Inverting input of the amplifier.
+IN	3	Non-inverting input of the amplifier.
V _{s-}	4	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V _{s+} and V _{s-} is from 5 V to 36 V.
NC	5	No Connection.
OUT	6	Amplifier output.
V _{s+}	7	Positive power supply. The voltage is from 5 V to 36 V. Split supplies are possible as long as the voltage between V _{s+} and V _{s-} is from 5 V to 36 V.

Pin Configuration (Top View)



PIN Name	SOIC-16L	SOIC-8L	Description
-IN A	1	2	Inverting input A of the amplifier.
+IN A	2	3	Non-inverting input of the amplifier.
V_{S-}	4	4	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 5 V to 36 V.
+IN B	6	5	Non-inverting input of the amplifier. This pin has the same voltage range as -IN B.
-IN B	7	6	Inverting input B of the amplifier. The voltage range is from ($V_{S-} - 0.1$ V) to ($V_{S+} - 1$ V).
OUT B	10	7	Amplifier B output.
V_{S+}	13	8	Positive power supply. The voltage is from 5 V to 36 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 5 V to 36 V.
OUT A	16	1	Amplifier A output.
NC	3, 5, 8, 9, 11, 12, 14, 15	-	No Connection.

Limiting Value

In accordance with the Absolute Maximum Rating System (IEC60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	40 V
Signal Input Terminals: Voltage	± 20 V
Signal Input Terminals: Current	Current Indefinite
Signal Differential Input Voltage	1.4 V
Output Short-Circuit	80 mA
Storage Temperature Range, T_{stg}	-65 °C to $+150$ °C
Junction Temperature, T_J	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	± 2000	V
Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	± 2000	V

Thermal Information

Thermal Metric	Package	Level	Unit
θ_{JA} Package Thermal Resistance	SOIC-8L	125	°C/W
	MSOP-8L	216	
	TSSOP-8L	160	
	SOIC-16L	95	

Electrical Characteristics

Unless otherwise noted, $T_A = 25^\circ\text{C}$, $V_S = \pm 15.0\text{ V}$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC PERFORMANCE						
Input Offset Voltage	V_{OS}			50	100	μV
Input Offset Voltage vs Temperature	dV_{OS} / dT	$T_A = -40^\circ\text{C}$ to 125°C		0.5		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B			± 50	± 100	nA
Input Offset Current	I_{OS}			± 40	± 100	nA
Open-loop voltage gain	A_{VOL}	$R_L \geq 2\text{ k}\Omega$, $V_O = 24\text{ V}_{p-p}$		135		dB
NOISE and DISTORTION PERFORMANCE						
Input Voltage Noise	E_N	f = 0.1 Hz to 10 Hz		0.2		μV_{p-p}
		f = 20 Hz to 20 kHz		4.5		μV_{p-p}
Input Voltage Noise Density	e_n	f = 10 Hz		7.5		$\text{nV}/\sqrt{\text{Hz}}$
		f = 100 Hz		5		$\text{nV}/\sqrt{\text{Hz}}$
		f = 1 kHz		3		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise Density	I_n	f = 10 Hz		1.6		$\text{pA}/\sqrt{\text{Hz}}$
		f = 100 Hz		0.8		$\text{pA}/\sqrt{\text{Hz}}$
		f = 1 kHz		0.7		$\text{pA}/\sqrt{\text{Hz}}$
Total Harmonic Distortion + Noise	THD+N	G = +5, f = 1 kHz, $V_O = 3\text{ V}_{RMS}$		0.0003 109		% dB
Intermodulation Distortion	IMD	G = +5, $V_O = 3\text{ V}_{RMS}$ SMPTE/DIN Two-Tone, 4:1 (60 Hz and 7 kHz)		0.0024 92.4		% dB
INPUT CHARACTERISTICS						
Input Common Mode Voltage Range	V_{CM}		± 11	± 12.3		V
Common Mode Rejection Rate	CMRR	$V_{CM} = \pm 11\text{ V}$		135		dB
DYNAMIC PERFORMANCE						
Gain-Bandwidth Product	GBP	f = 10 kHz		82		MHz
		f = 1 MHz		33		
Slew Rate	SR	$A_V = 5.7$, $V_O = 20\text{ V}_{pp}$		17		$\text{V}/\mu\text{s}$
Full Power Bandwidth	PBW	$A_V = 5$		1.2		MHz
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_{OUT}	$R_L = 2\text{ k}\Omega$, $A_{VOL} \geq 120\text{ dB}$, $V_S \geq \pm 5\text{ V}$	V_{S+} 1.5		V_{S-} 1.5	V
		$R_L = 2\text{ k}\Omega$, $A_{VOL} \geq 110\text{ dB}$, $V_S < \pm 5\text{ V}$	V_{S+} 1.5		V_{S-} 1.5	
Short-circuit Current	I_{SOURCE}	Open loop, $V_{in} = \pm 200\text{ mV}$, No load		70		mA
	I_{SINK}			-70		
POWER SUPPLY						
Operating Supply Voltage	V_S	$T_A = -40$ to $+125^\circ\text{C}$	5		36	V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{ V}$ to $\pm 10\text{ V}$		130		dB
Quiescent Current (Per amplifier)	I_Q			3.3	4	mA

Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, unless otherwise noted.

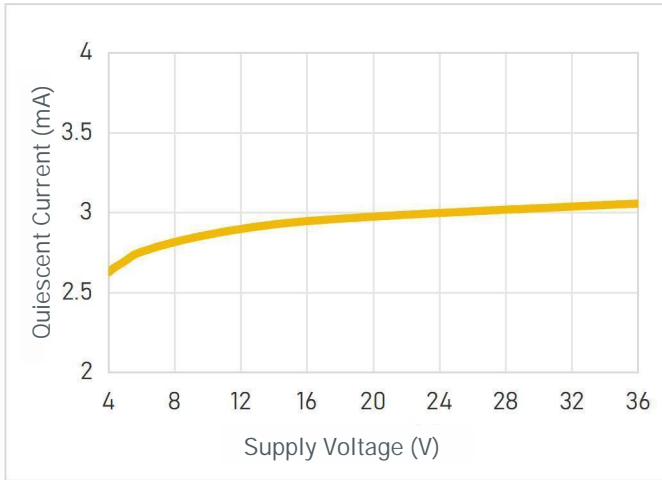


Figure 1. Quiescent Current vs Supply Voltage

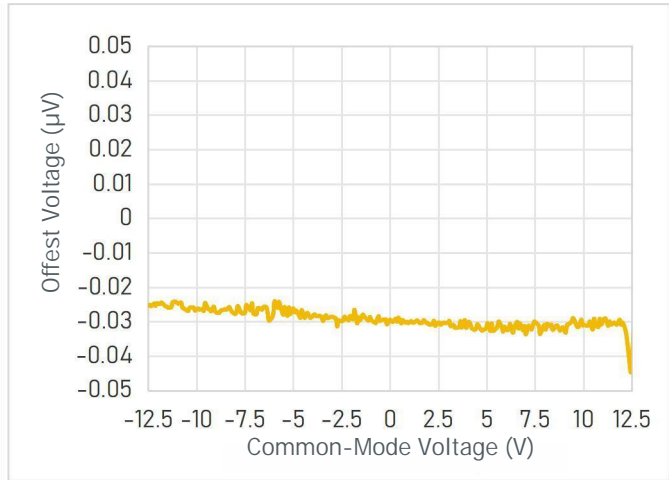


Figure 2. Offset Voltage vs Common-Mode Voltage

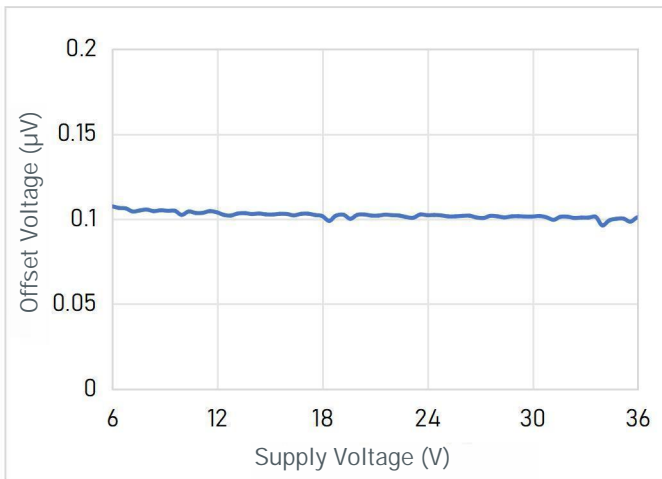


Figure 3. Offset Voltage vs Supply Voltage

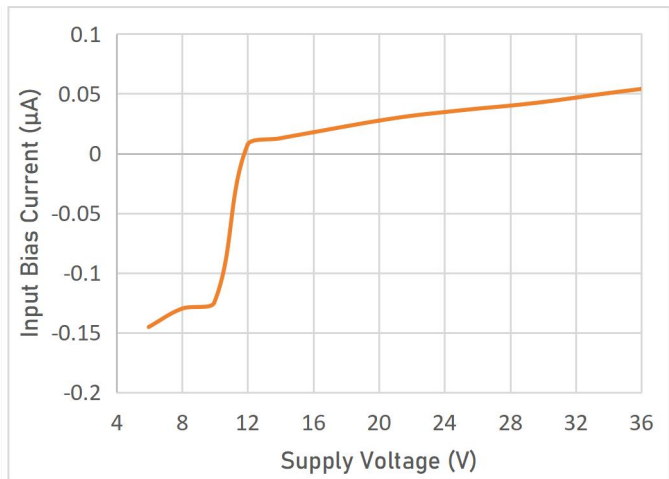


Figure 4. Input Bias Current vs Supply Voltage

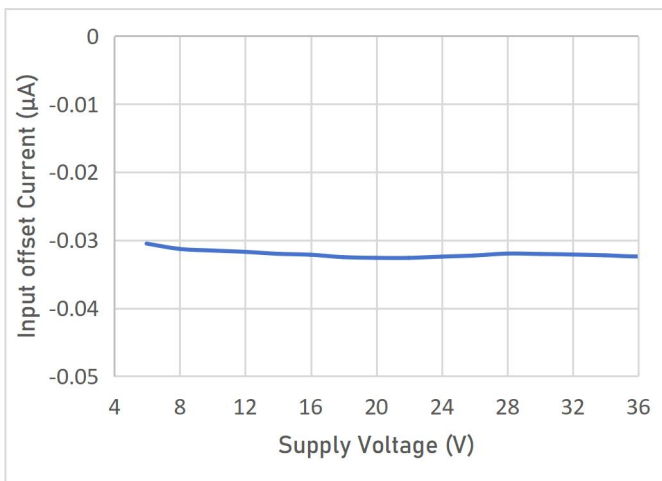


Figure 5. Input Offset Current vs Supply Voltage

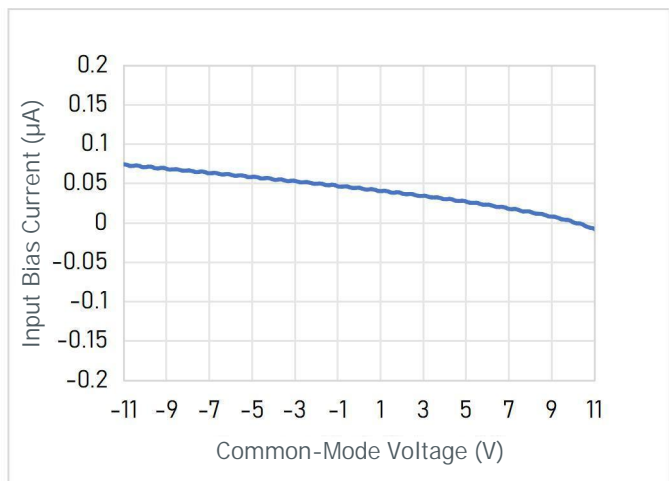


Figure 6. Input Bias Current vs Common-Mode Voltage

Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

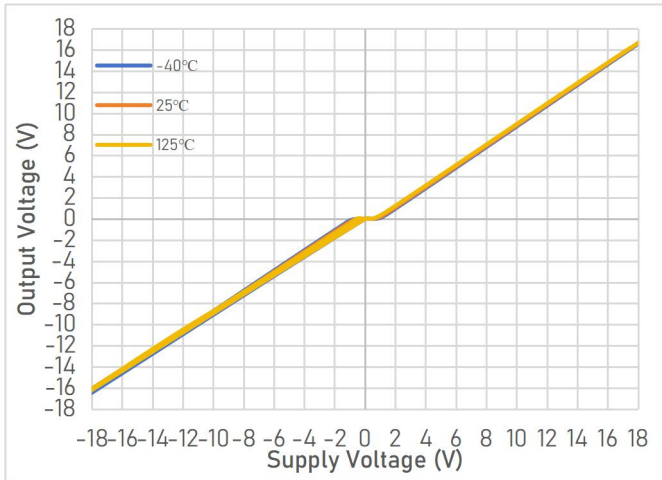


Figure 7. Output Voltage vs Supply Voltage

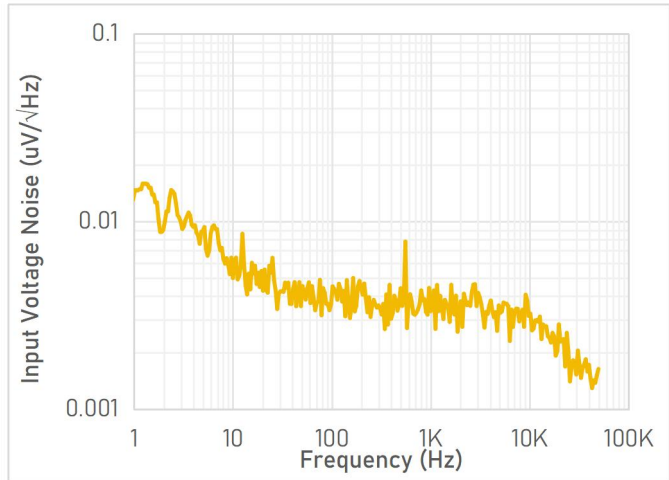


Figure 8. Input Voltage Noise vs Frequency

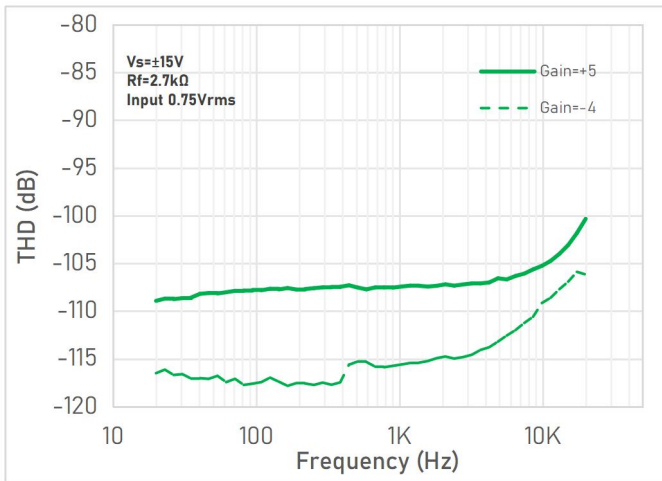


Figure 9. Total Harmonic Distortion vs Frequency

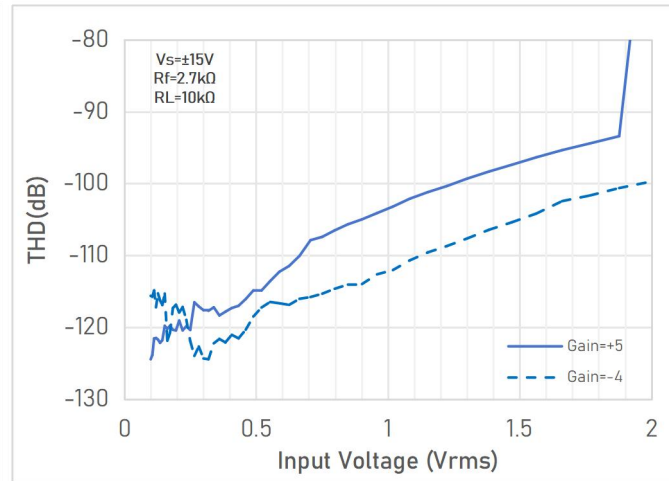


Figure 10. Total Harmonic Distortion vs Input Voltage

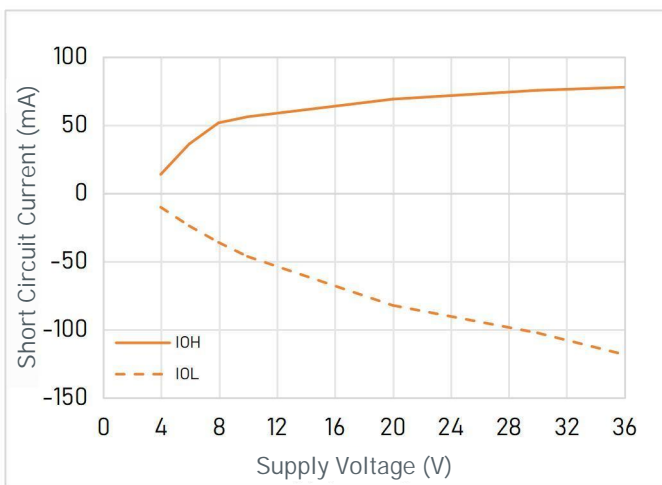


Figure 11. Short Circuit Current vs Supply Voltage

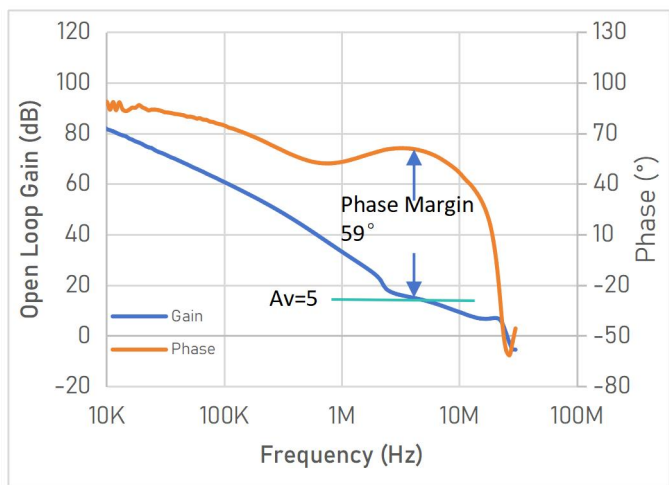


Figure 12. Open Loop Gain and Phase vs Frequency

Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, unless otherwise noted.

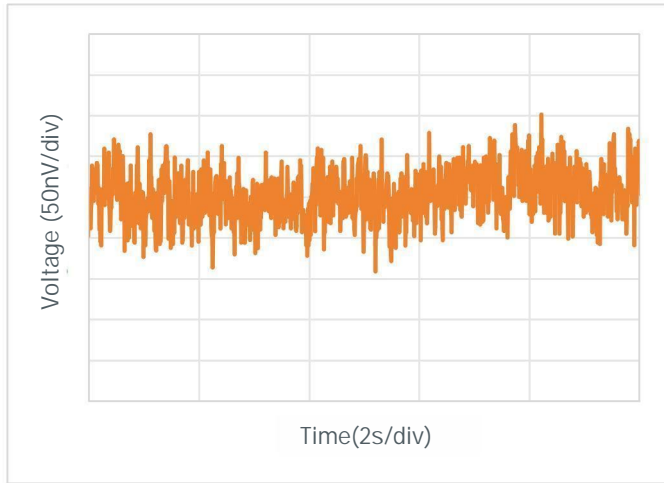


Figure 13. Low Frequency Noise (0.1-10Hz)

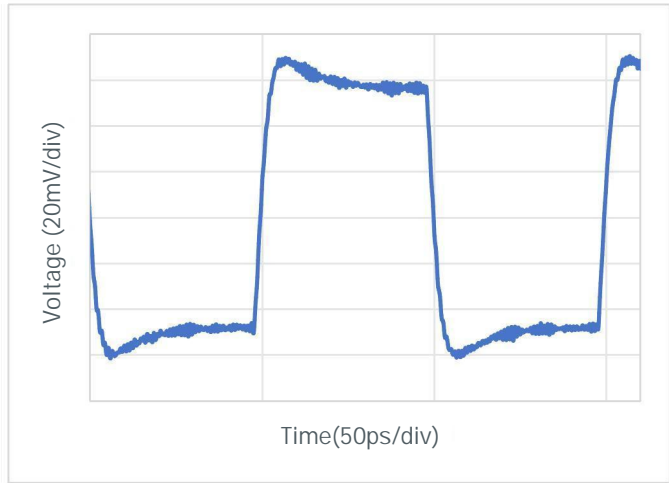


Figure 14. Small-Signal Transient Response

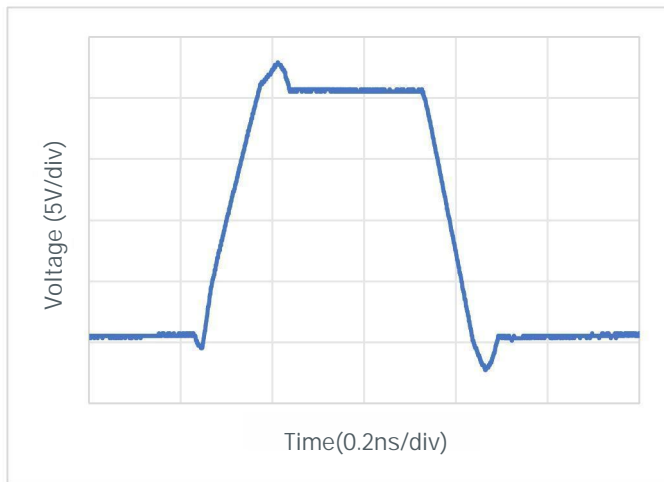


Figure 15. Large-Signal Transient Response

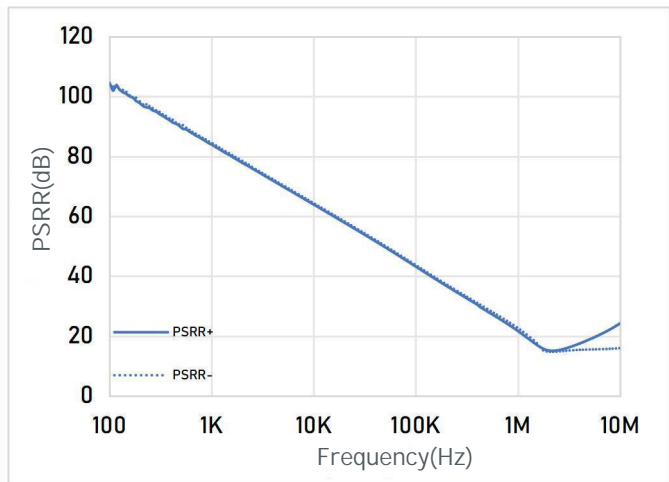


Figure 16. PSRR vs Frequency

Application Notes

LTA37 Series Op-Amps could be a good replacement of OP27, OP200 with or without removal of external compensation or nulling components. Additionally, the LTA37 may be fitted to unnullled 741 type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct LTA37 operation. LTA37 offset voltage may be nulled to zero (or other desired setting) using a potentiometer. The LTA37 provides stable operation with load capacitances of up to 1000 pF and $\pm 10V$ swings; larger capacitances should be decoupled with a 50 Ω resistor inside the feedback loop. Closed loop gain must be at least five. For gains above ten, the LTA37 has a clear advantage over the unity stable OP27.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

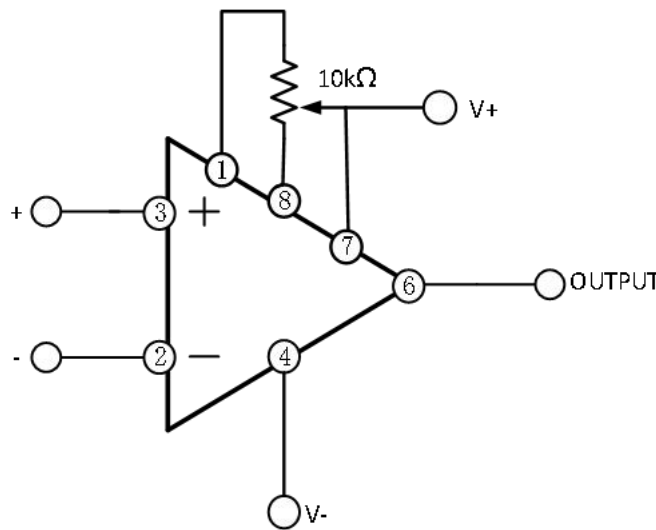


Figure 17 Offset Nulling Circuit

Offset Voltage Adjustment

The input offset voltage of the LTA37 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10 k Ω trim potentiometer may be used. TCV_{OS} is not degraded (see offset nulling circuit). Other potentiometer values from 1 k Ω to 1 M Ω can be used with a slight degradation (0.1 $\mu V/^{\circ}C$ to 0.2 $\mu V/^{\circ}C$) of TCV_{OS} . Trimming to a value other than zero creates a drift of approximately $(V_{OS}/300) \mu V/^{\circ}C$. For example, the change in TCV_{OS} will be 0.33 $\mu V/^{\circ}C$ if V_{OS} is adjusted to 100 μV . The offset voltage adjustment range with a 10 k Ω potentiometer is ± 4 mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjunction with fixed resistors. For example, the network shown in figure 18 will have a $\pm 280 \mu V$ adjustment range.

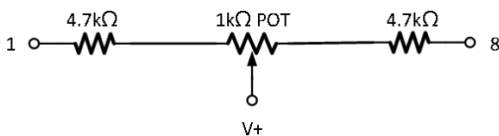


Figure 18 Offset Voltage Adjustment

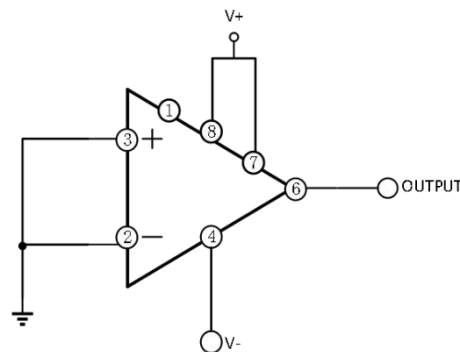
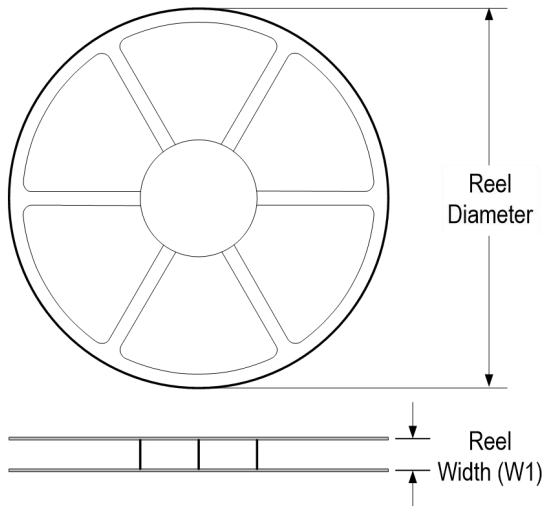


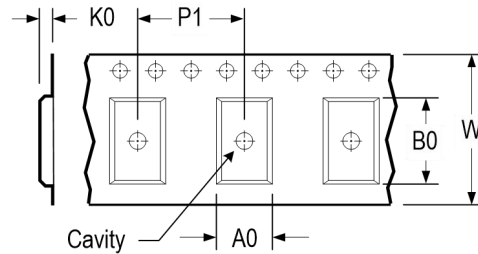
Figure 19 Burn-In Circuit

Tape and Reel Information

REEL DIMENSIONS

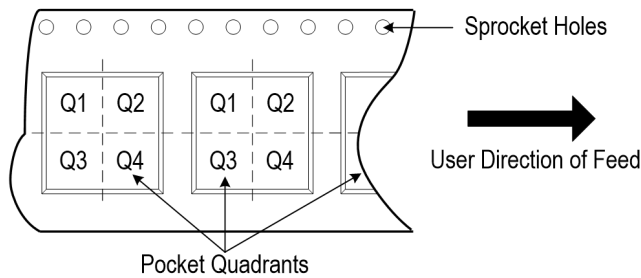


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

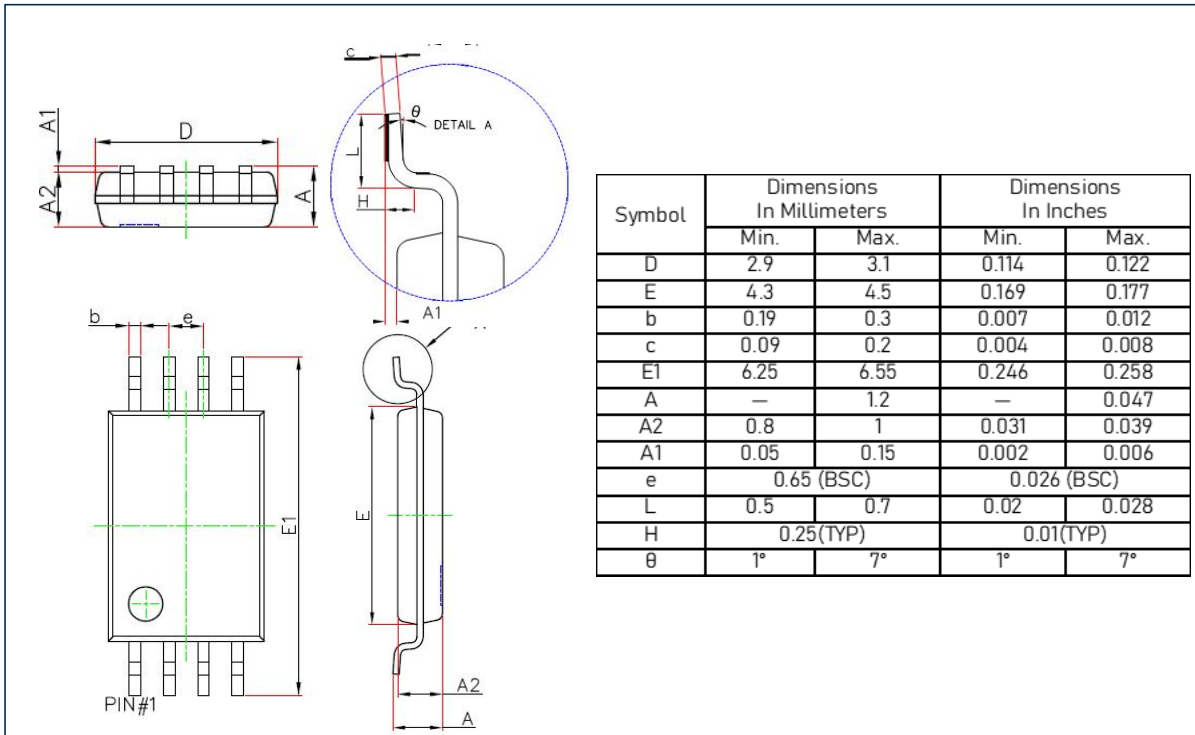


* All dimensions are nominal

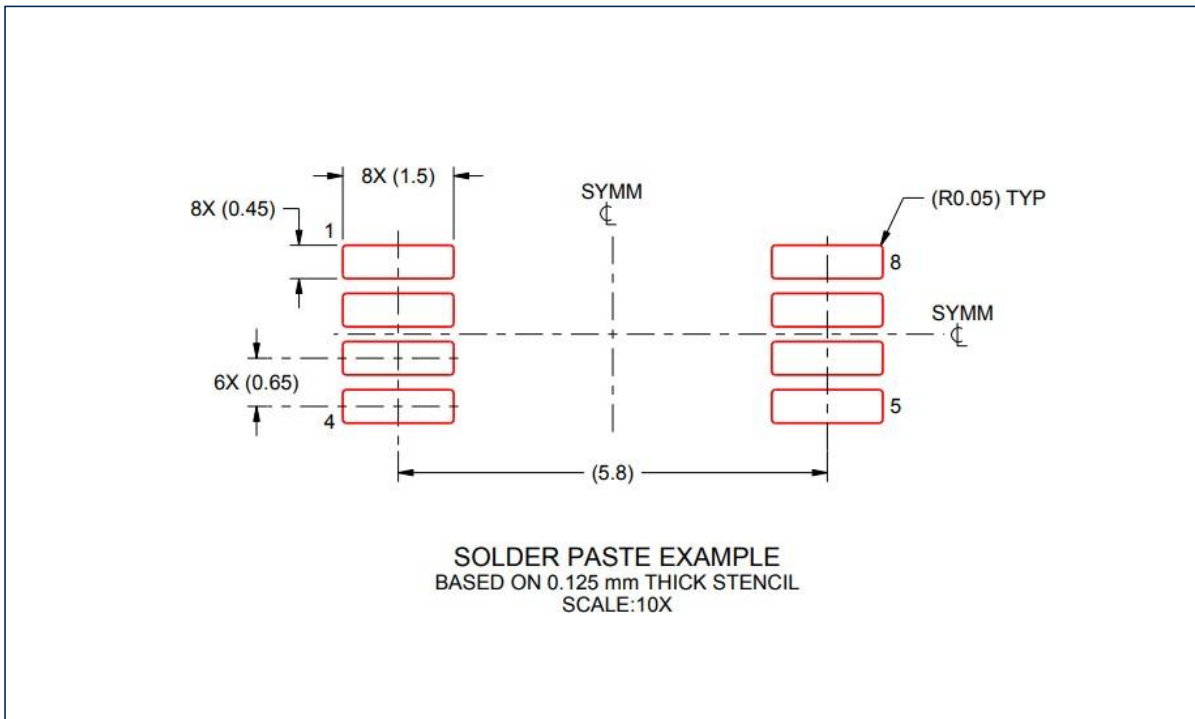
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA37XS8/R8	SOIC	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTA37XT8/R8	TSSOP	8	4 000	330	12.5	6.5	4.0	1.2	8.0	12.0	Q1
LTA37XV8/R6	MSOP	8	3 000	330	12.5	5.0	3.5	2.0	8.0	12.0	Q1
LTA37JXS8/R8	SOIC	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTA37JXT8/R8	TSSOP	8	4 000	330	12.5	6.5	4.0	1.2	8.0	12.0	Q1
LTA37JXV8/R6	MSOP	8	3 000	330	12.5	5.0	3.5	2.0	8.0	12.0	Q1
LTA237XS8/R8	SOIC	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTA237XS16/R5	SOIC	16	2 500	330	16.5	6.6	10.4	2.0	8.0	16.0	Q1

Package Outlines

DIMENSIONS, TSSOP-8L

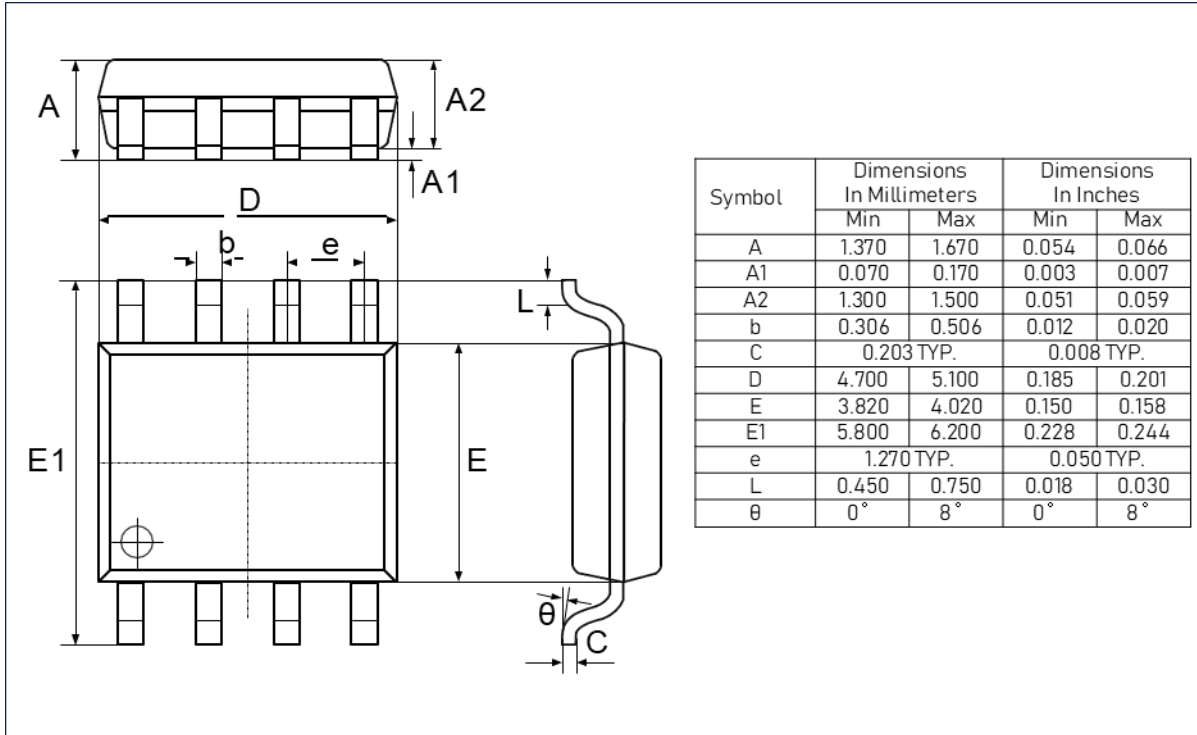


RECOMMENDED SOLDERING FOOTPRINT, TSSOP-8L

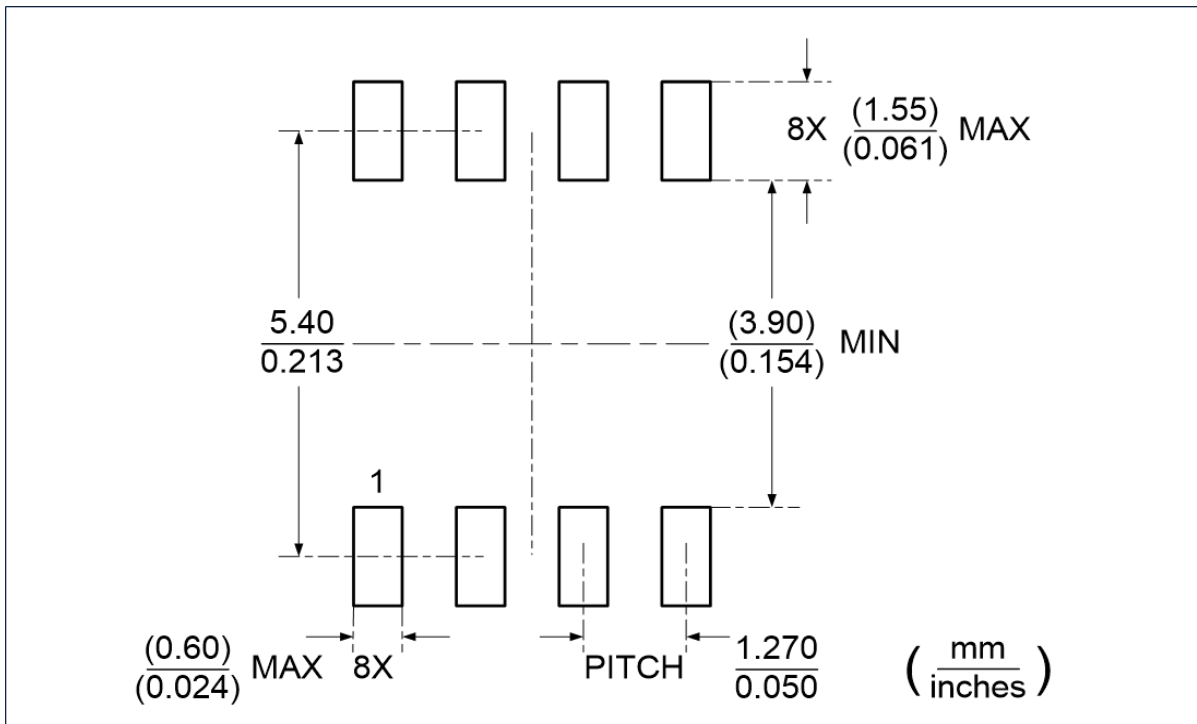


Package Outlines (cont.)

DIMENSIONS, SOIC-8L

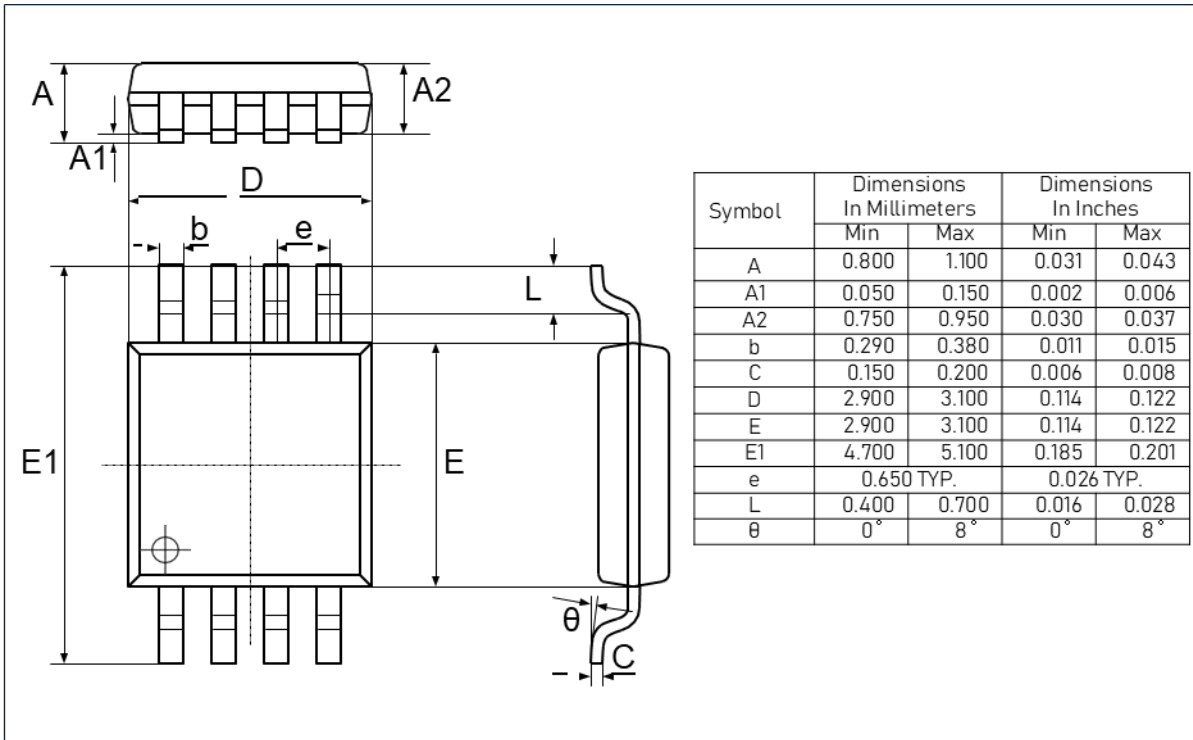


RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L

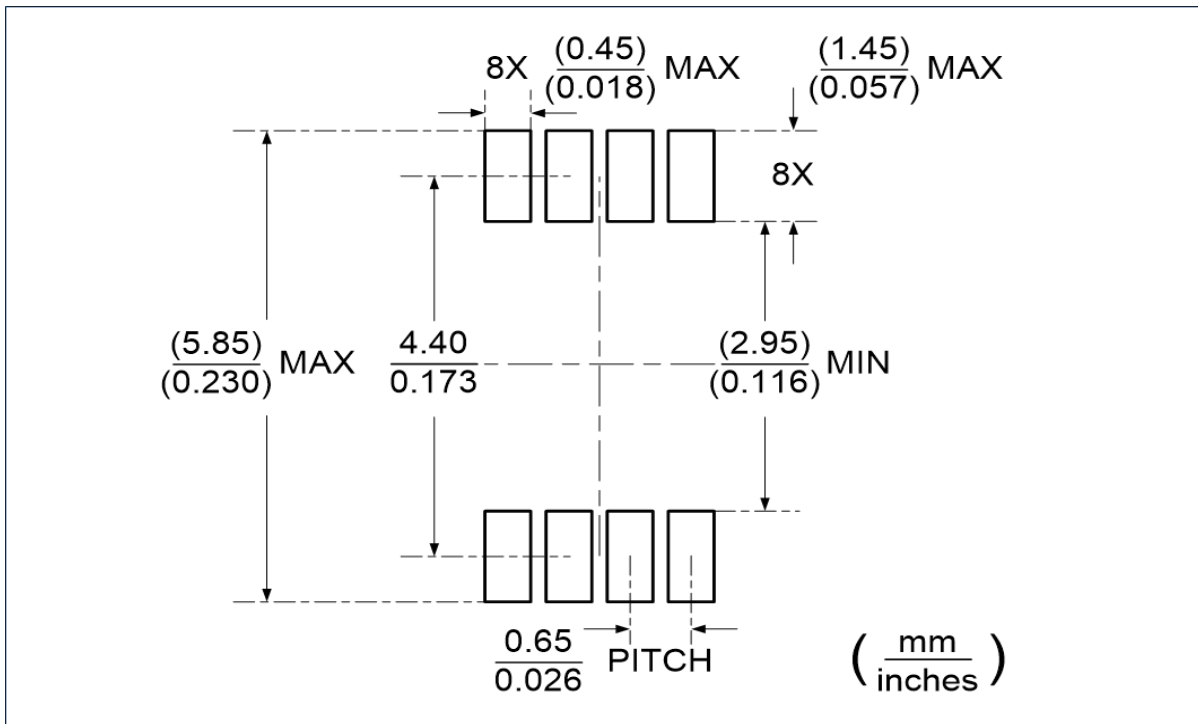


Package Outlines (cont.)

DIMENSIONS, MSOP-8L

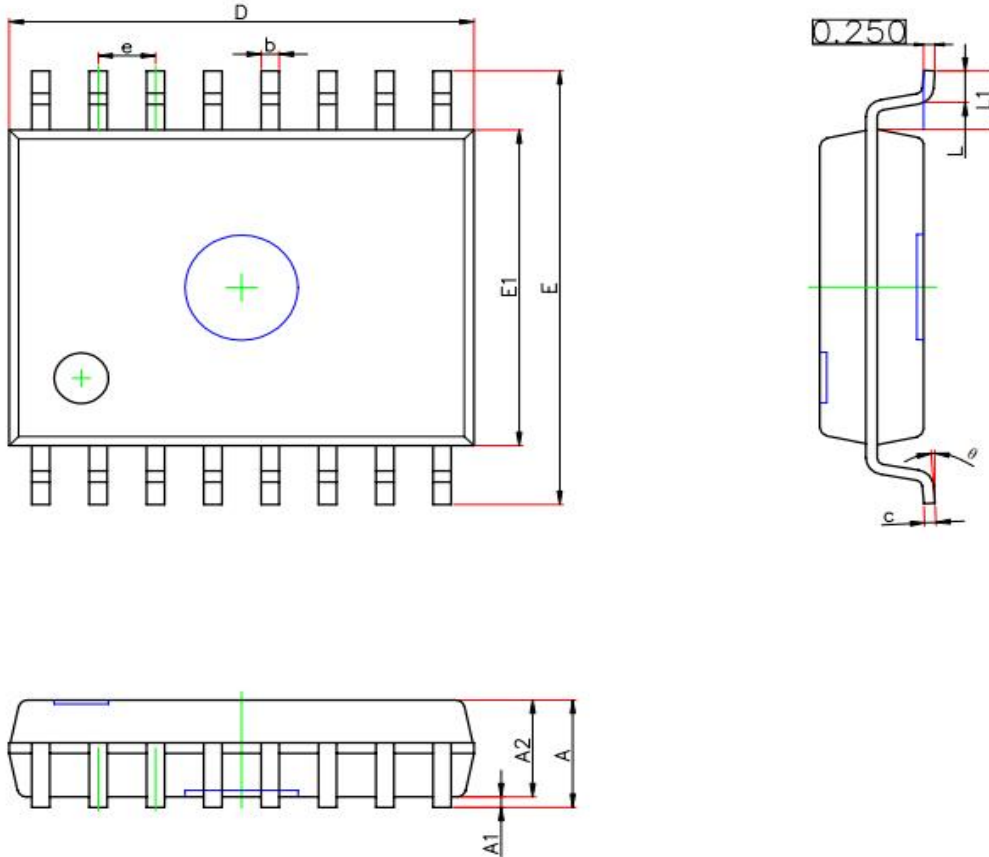


RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



Package Outlines (Cont.)

DIMENSIONS, SOIC-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	-	2.650	-	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.350	0.430	0.014	0.017
c	0.240	0.290	0.009	0.011
D	10.200	10.400	0.402	0.409
E	10.100	10.500	0.398	0.413
E1	7.400	7.600	0.291	0.299
e	1.270(BSC)		0.050(BSC)	
L	0.550	0.850	0.022	0.033
L1	1.400(REF)		0.060(REF)	
θ	0°	8°	0°	8°

Precision, Low Noise, High Speed Operational Amplifier ($A_{VCL} \geq 5$)

Important Notice

Linearin is a global fabless semiconductor company specializing in advanced high-performance high-quality analog/mixed-signal IC products and sensor solutions. The company is devoted to the innovation of high performance, analog-intensive sensor front-end products and modular sensor solutions, applied in multi-market of medical & wearable devices, smart home, sensing of IoT, intelligent industrial & smart factory (industry 4.0), and automotives. Linearin's product families include widely-used standard catalog products, solution-based application specific standard products (ASSPs) and sensor modules that help customers achieve faster time-to-market products. Go to <http://www.linearin.com> for a complete list of Linearin product families.

For additional product information, or full datasheet, please contact with the Linearin's Sales Department or Representatives.