

### General Description

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The LTA805x family is true single-supply voltage feedback operational amplifiers feature high speed performance with 200 MHz of small signal bandwidth and 160 V/ $\mu$ s slew rate. The products are specified for 3.3 V and 5 V supplies, input common mode voltage range extends to 0.1 V below  $V_{S-}$  and 1 V from  $V_{S+}$ , and output voltage range extends to power rail, allowing wide dynamic range especially desirable in low voltage applications. The LTA805x also offer excellent signal quality of low distortion and fast settling time (13.5 ns to 0.1%), which make them ideal as buffers to single-supply ADCs.

Operating on supplies from +3.3 V to +6.6 V and dual supplies up to  $\pm$ 3.3 V, the LTA805x are ideal for a wide range of applications, from battery-operated systems with large bandwidth requirements to high speed systems where component density requires lower power dissipation. The single version LTA8051 device is available in micro-size SOT23-5L and SOIC-8L packages. The dual LTA8052 device is offered in MSOP-8L and SOIC-8L packages. The quad LTA8054 device is offered in SOIC-14L and TSSOP-14L packages.

### Features and Benefits

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- High Speed and Fast Settling on 5 V
- 200 MHz,  $-3$  dB bandwidth ( $G = +1$ )
- 160 V/ $\mu$ s slew rate
- 13.5 ns settling time to 0.1%
- Fully specified at 3.3 V and 5 V Supplies
- Input Common Mode Voltage 0.1 V Beyond  $V_{S-}$ , 1 V from  $V_{S+}$
- Output Short Circuit Current 120 mA
- Operating Temperature Range  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

### Applications

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- Photodiode Amplification
- Video Buffer
- Active Filters
- Driving A/D Converters
- Motor Phase Current Sense
- Portable Equipment
- Battery-Powered Instrumentation

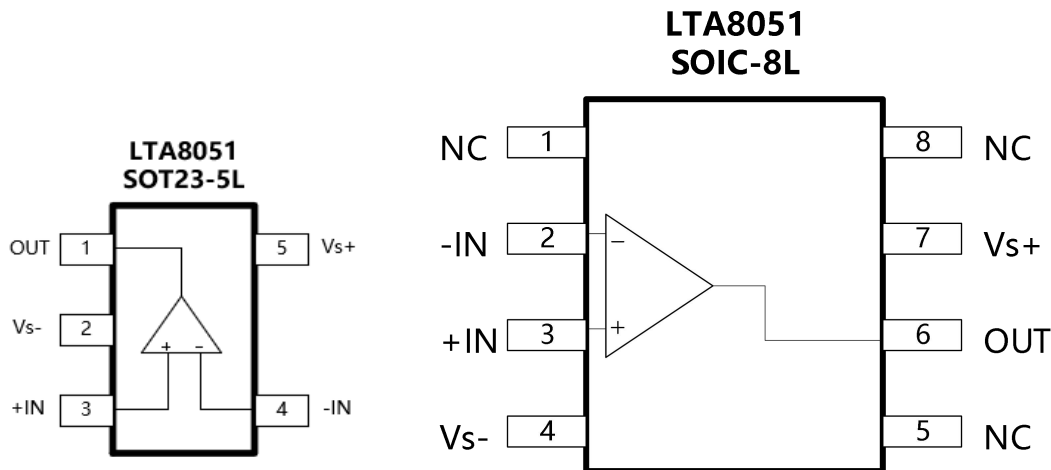
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### Ordering Information

Part Number	Package Type	Package Quantity	ECO Class	Mark Code
LTA8051XT5/R6	SOT23-5L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	W57, W51
LTA8051XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	W8051, W6051
LTA8052XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	W8052, W6052
LTA8052XV8/R6	MSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	W8052, W6052
LTA8054XS14/R5	SOIC-14L	Tape and Reel, 2 500	Green (RoHS & no Sb/Br)	W8054, W6054
LTA8054XT14/R6	TSSOP-14L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	W8054, W6054

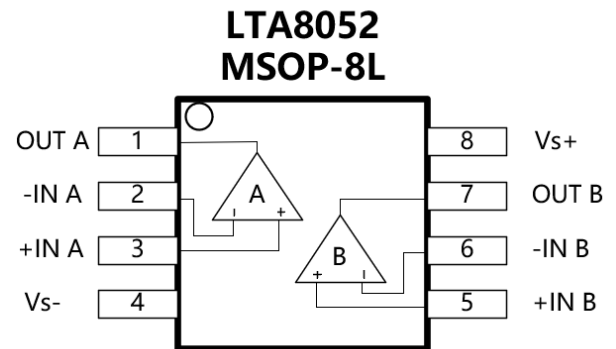
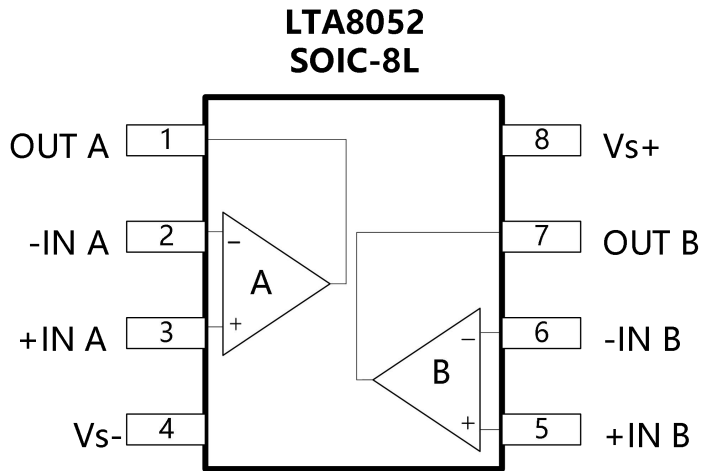
### Pin Configuration (Top View)



PIN Name	SOT23-5L	SOIC-8L	Description
OUT	1	6	Amplifier output.
$V_{s-}$	2	4	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between $V_{s+}$ and $V_{s-}$ is from 3.3 V to 6.6 V.
+IN	3	3	Non-inverting input of the amplifier. The voltage range is from ( $V_{s-} - 0.1$ V) to ( $V_{s+} - 1$ V).
-IN	4	2	Inverting input of the amplifier. This pin has the same voltage range as -IN.
$V_{s+}$	5	7	Positive power supply. The voltage is from 3.3 V to 6.6 V. Split supplies are possible as long as the voltage between $V_{s+}$ and $V_{s-}$ is from 3.3 V to 6.6 V.
NC	-	1, 5, 8	No Connection

# LTA8051, LTA8052, LTA8054

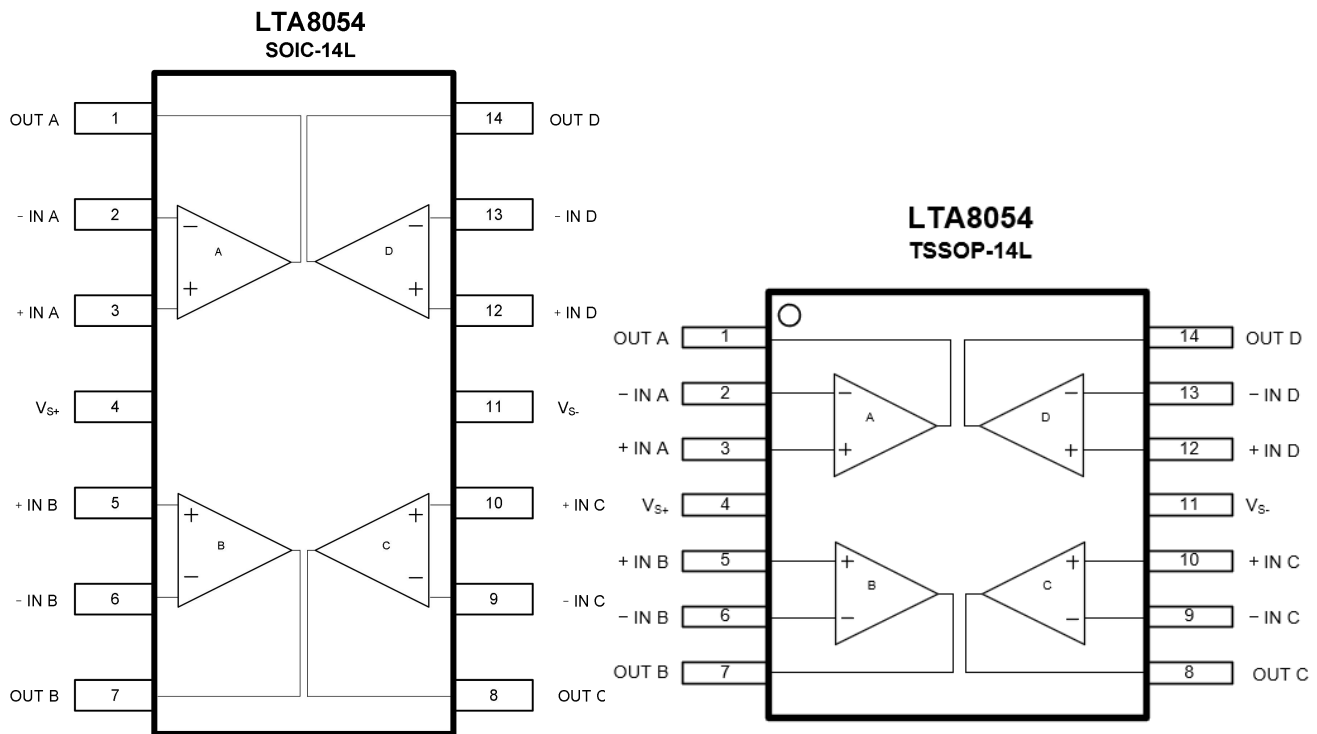
## 200 MHz, High Slew Rate, RRO, CMOS Amplifiers



PIN Name	SOIC-8L / MSOP-8L	Description
OUT A	1	Amplifier A output.
-IN A	2	Inverting input A of the amplifier. The voltage range is from $(V_{S-} - 0.1\text{ V})$ to $(V_{S+} - 1\text{ V})$ .
+IN A	3	Non-inverting input of the amplifier. This pin has the same voltage range as -IN A.
$V_{S-}$	4	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 3.3 V to 6.6 V.
+IN B	5	Non-inverting input of the amplifier. This pin has the same voltage range as -IN B.
-IN B	6	Inverting input B of the amplifier. The voltage range is from $(V_{S-} - 0.1\text{ V})$ to $(V_{S+} - 1\text{ V})$ .
OUT B	7	Amplifier B output.
$V_{S+}$	8	Positive power supply. The voltage is from 3.3 V to 6.6 V. Split supplies are possible as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 3.3 V to 6.6 V.

# LTA8051, LTA8052, LTA8054

## 200 MHz, High Slew Rate, RRO, CMOS Amplifiers



PIN Name	SOIC-14L / TSSOP-14L	Description
OUT A	1	Amplifier A output.
-IN A	2	Inverting input A of the amplifier. The voltage range is from ( $V_{S-} - 0.1\text{ V}$ ) to ( $V_{S+} - 1\text{ V}$ ).
+IN A	3	Non-inverting input of the amplifier. This pin has the same voltage range as -IN A.
$V_{S+}$	4	Positive power supply. The voltage is from 3.3 V to 6.6 V. Split supplies are possible as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 3.3 V to 6.6 V.
+IN B	5	Non-inverting input of the amplifier. This pin has the same voltage range as -IN B.
-IN B	6	Inverting input B of the amplifier. The voltage range is from ( $V_{S-} - 0.1\text{ V}$ ) to ( $V_{S+} - 1\text{ V}$ ).
OUT B	7	Amplifier B output.
OUT C	8	Amplifier C output.
-IN C	9	Inverting input C of the amplifier. The voltage range is from ( $V_{S-} - 0.1\text{ V}$ ) to ( $V_{S+} - 1\text{ V}$ ).
+IN C	10	Non-inverting input of the amplifier. This pin has the same voltage range as -IN C.
$V_{S-}$	11	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 3.3 V to 6.6 V.
+IN D	12	Non-inverting input of the amplifier. This pin has the same voltage range as -IN D.
-IN D	13	Inverting input D of the amplifier. The voltage range is from ( $V_{S-} - 0.1\text{ V}$ ) to ( $V_{S+} - 1\text{ V}$ ).
OUT D	14	Amplifier D output.

### Limiting Value

In accordance with the Absolute Maximum Rating System (IEC60134).

Parameter	Absolute Maximum Rating
Supply Voltage, $V_{S+}$ to $V_{S-}$	10 V
Signal Input Terminals: Voltage	$V_{S-} - 0.5$ V to $V_{S+} + 0.5$ V
Signal Input Terminals: Current	$\pm 10$ mA
Output Short-Circuit	Continuous
Storage Temperature Range, $T_{stg}$	$-65$ °C to $+150$ °C
Junction Temperature, $T_j$	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

### ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	$\pm 8\ 000$	V
Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	$\pm 1\ 000$	V

### Thermal Information

Thermal Metric	Package	Level	Unit
$\theta_{JA}$ Package Thermal Resistance	SOT23-5L	190	°C/W
	SOIC-8L	125	
	MSOP-8L	216	
	TSSOP-14L	112	
	SOIC-14L	115	

### 5 V Electrical Characteristics

Unless otherwise noted,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $A_V = +1$ ,  $R_F = 20\ \Omega$ ;  $A_V \geq +2$ ,  $R_F = 470\ \Omega$  and  $R_L = 100\ \Omega$ .

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>DYNAMIC PERFORMANCE</b>						
-3dB Small-Signal Bandwidth	$f_{-3dB}$	$G = +1$ , $V_{OUT} = 0.2\text{ V}_{P-P}$ , $R_F = 20\ \Omega$ , $R_L = 150\ \Omega$		200		MHz
		$G = +1$ , $V_{OUT} = 0.2\text{ V}_{P-P}$ , $R_F = 20\ \Omega$ , $R_L = 1\text{ k}\Omega$		240		
		$G = +2$ , $V_{OUT} = 0.2\text{ V}_{P-P}$ , $R_F = 470\ \Omega$ , $R_L = 150\ \Omega$		85		
		$G = +2$ , $V_{OUT} = 0.2\text{ V}_{P-P}$ , $R_F = 470\ \Omega$ , $R_L = 1\text{ k}\Omega$		110		
Gain-Bandwidth Product	GBP	$G = +10$ , $R_L = 150\ \Omega$		120		MHz
		$G = +10$ , $R_L = 1\text{ k}\Omega$		125		
Bandwidth for 0.1dB Flatness	$f_{0.1dB}$	$G = +2$ , $V_{OUT} = 0.2\text{ V}_{P-P}$ , $R_F = 470\ \Omega$ , $R_L = 150\ \Omega$		8		MHz
Slew Rate	SR	$G = +1$ , $V_{IN} = 2\text{ V}_{P-P}$		160/180		V/ $\mu\text{s}$
Rise Time	$T_r$	$G = +1$ , $V_{IN} = 0.2\text{ V Step}$		2.2		ns
Fall Time	$T_f$	$G = +1$ , $V_{IN} = 0.2\text{ V Step}$		1.8		ns
Settling Time to 0.1%	$T_s$	$G = -1$ , $R_F = 402\ \Omega$ , $V_{OUT} = 2\text{ V Step}$		13.5		ns
<b>NOISE and DISTORTION PERFORMANCE</b>						
Input Voltage Noise Density	$e_n$	$f \geq 1\text{ MHz}$		1		nV/ $\sqrt{\text{Hz}}$
Differential Gain	DG	$G = +2$ , $R_L = 150\ \Omega$		0.05		%
Differential Phase	DP	$G = +2$ , $R_L = 150\ \Omega$		0.05		°
<b>DC PERFORMANCE</b>						
Input Offset Voltage	$V_{OS}$			$\pm 1.8$	$\pm 15$	mV
Input Offset Voltage vs Temperature	$dV_{OS} / dT$	$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		4		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$			0.5		pA
Input Offset Current	$I_{OS}$			0.2		pA
Open-loop voltage gain	$A_{VOL}$	$R_L = 100\ \Omega$ , $V_O = 3.3\text{ V}_{P-P}$		80	100	dB
<b>INPUT CHARACTERISTICS</b>						
Input Common Mode Voltage Range	$V_{CM}$		$V_{S-} - 0.1$		$V_{S+} - 1$	V
Common Mode Rejection Rate	CMRR	$G = +100$ , $V_{CM} = -2.2\text{ V to } +1\text{ V}$	60	80	108	dB
<b>OUTPUT CHARACTERISTICS</b>						
High Output Voltage Swing	$V_{OH}$	No Load	$V_{S+} - 80$	$V_{S+} - 40$		mV
		$R_L = 100\ \Omega$	$V_{S+} - 450$	$V_{S+} - 350$		
Low Output Voltage Swing	$V_{OL}$	No Load		$V_{S-} + 5$	$V_{S-} + 20$	mV
		$R_L = 100\ \Omega$		$V_{S-} + 100$	$V_{S-} + 250$	
Short-circuit Current	$I_{SOURCE}$	Open loop, $V_{IN} = \pm 200\text{ mV}$		120		mA
	$I_{SINK}$			140		
<b>POWER SUPPLY</b>						
Operating Supply Voltage	$V_S$	$T_A = -40\text{ to } +125\ ^\circ\text{C}$	3.3		6.6	V
Quiescent Current (Per amplifier)	$I_Q$			6.7	8	mA

### 3.3 V Electrical Characteristics

Unless otherwise noted,  $V_S = \pm 1.65\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $A_V = +1$ ,  $R_F = 20\ \Omega$ ;  $A_V \geq +2$ ,  $R_F = 470\ \Omega$  and  $R_L = 100\ \Omega$ .

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>DYNAMIC PERFORMANCE</b>						
-3dB Small-Signal Bandwidth	$f_{-3dB}$	$G = +1$ , $V_{OUT} = 0.2\ V_{P-P}$ , $R_F = 20\ \Omega$ , $R_L = 150\ \Omega$		160		MHz
		$G = +1$ , $V_{OUT} = 0.2\ V_{P-P}$ , $R_F = 20\ \Omega$ , $R_L = 1\ \text{k}\Omega$		200		
		$G = +2$ , $V_{OUT} = 0.2\ V_{P-P}$ , $R_F = 470\ \Omega$ , $R_L = 150\ \Omega$		80		
		$G = +2$ , $V_{OUT} = 0.2\ V_{P-P}$ , $R_F = 470\ \Omega$ , $R_L = 1\ \text{k}\Omega$		105		
Gain-Bandwidth Product	GBP	$G = +10$ , $R_L = 150\ \Omega$		120		MHz
		$G = +10$ , $R_L = 1\ \text{k}\Omega$		125		
Bandwidth for 0.1dB Flatness	$f_{0.1dB}$	$G = +2$ , $V_{OUT} = 0.2\ V_{P-P}$ , $R_F = 470\ \Omega$ , $R_L = 150\ \Omega$		7		MHz
Slew Rate	SR	$G = +1$ , $V_{IN} = 2\ V_{P-P}$		150/170		V/ $\mu\text{s}$
Rise Time	$T_r$	$G = +1$ , $V_{IN} = 0.2\ \text{V Step}$		4		ns
Fall Time	$T_f$	$G = +1$ , $V_{IN} = 0.2\ \text{V Step}$		4		ns
Settling Time to 0.1%	$T_s$	$G = -1$ , $R_F = 402\ \Omega$ , $V_{OUT} = 2\ \text{V Step}$		16.5		ns
<b>NOISE and DISTORTION PERFORMANCE</b>						
Input Voltage Noise Density	$e_n$	$f \geq 1\ \text{MHz}$		1		nV/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE</b>						
Input Offset Voltage	$V_{OS}$			$\pm 1.5$	$\pm 15$	mV
Input Offset Voltage vs Temperature	$dV_{OS} / dT$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$			0.6		pA
Input Offset Current	$I_{OS}$			0.6		pA
Open-loop voltage gain	$A_{VOL}$	$R_L = 100\ \Omega$ , $V_O = 1.8\ V_{P-P}$		70	80	dB
<b>INPUT CHARACTERISTICS</b>						
Input Common Mode Voltage Range	$V_{CM}$		$V_{S-} - 0.1$		$V_{S+} - 1$	V
Common Mode Rejection Rate	CMRR	$G = +100$ , $V_{CM} = -1.65\ \text{V}$ to $+0.35\ \text{V}$	55	60	90	dB
<b>OUTPUT CHARACTERISTICS</b>						
High Output Voltage Swing	$V_{OH}$	No Load	$V_{S+} - 50$	$V_{S+} - 30$		mV
		$R_L = 100\ \Omega$	$V_{S+} - 350$	$V_{S+} - 300$		
Low Output Voltage Swing	$V_{OL}$	No Load		$V_{S-} + 3$	$V_{S-} + 5$	mV
		$R_L = 100\ \Omega$		$V_{S-} + 180$	$V_{S-} + 200$	
Short-circuit Current	$I_{SOURCE}$	Open loop, $V_{IN} = \pm 200\ \text{mV}$		70		mA
	$I_{SINK}$			90		
<b>POWER SUPPLY</b>						
Operating Supply Voltage	$V_S$	$T_A = -40$ to $+125\ ^\circ\text{C}$	3.3		6.6	V
Quiescent Current (Per amplifier)	$I_Q$			6.3	7	mA

Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $R_F = 20\ \Omega$  for  $G = +1$ ,  $R_F = 470\ \Omega$  for  $G = +2$ ,  $G = +10$ , and  $R_L = 150\ \Omega$ , unless otherwise noted.

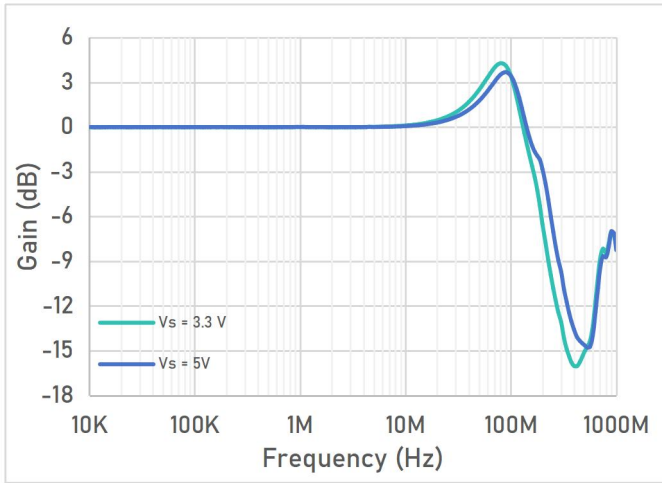


Figure 1. Closed-loop Bandwidth ( $G = +1$ )

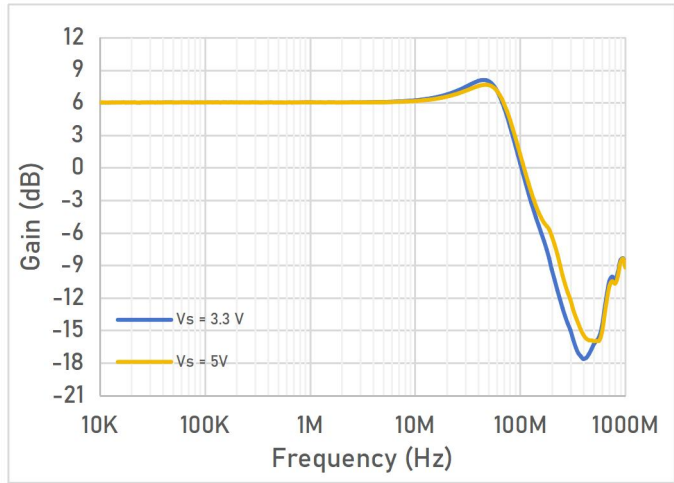


Figure 2. Closed-loop Bandwidth ( $G = +2$ )

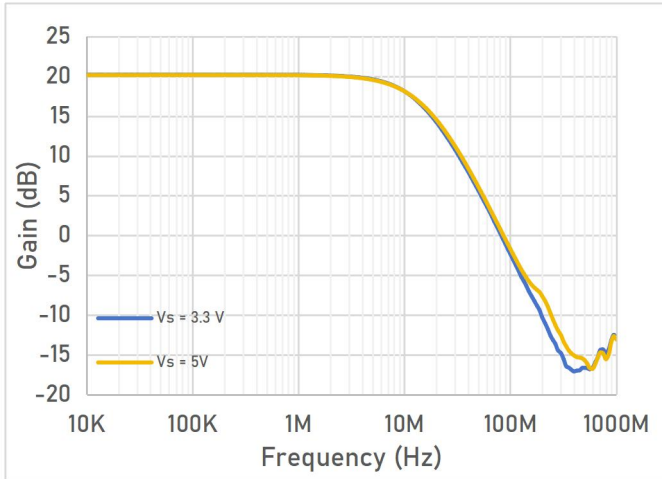


Figure 3. Closed-loop Bandwidth ( $G = +10$ )

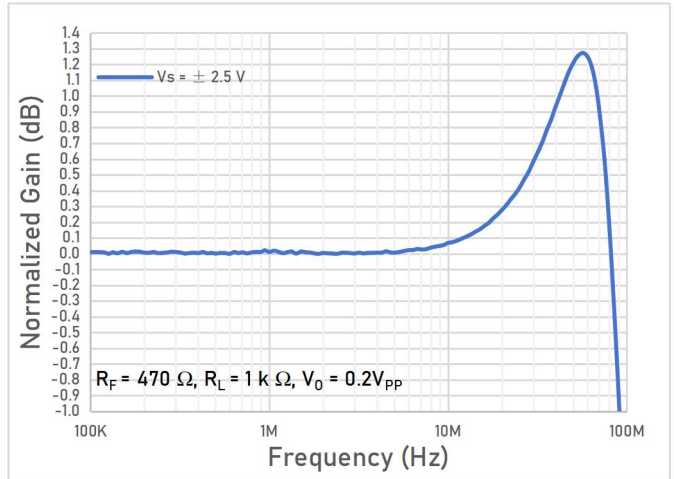


Figure 4. 0.1 dB Gain Flatness ( $G = +2$ )

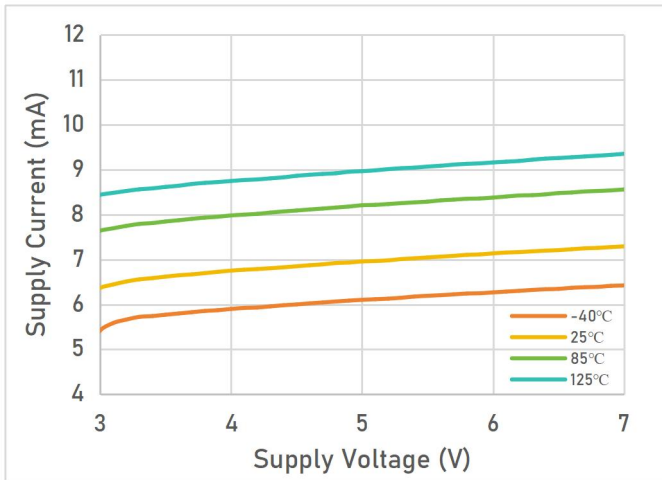


Figure 5. Supply Current per Channel vs Supply Voltage

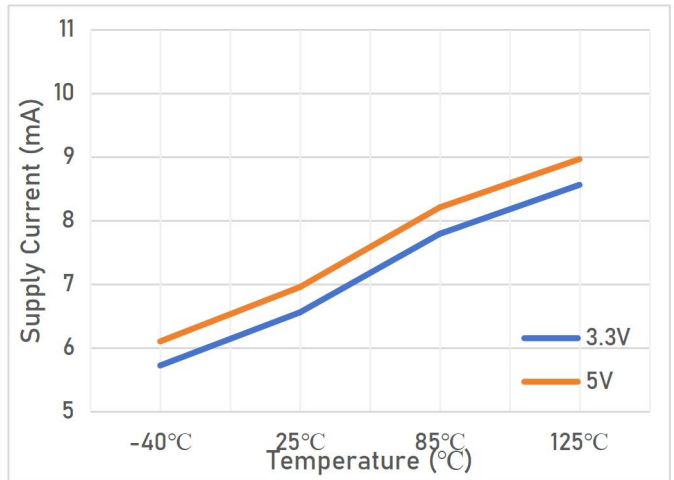


Figure 6. Supply Current per Channel vs Temperature

Typical Characteristics (cont.)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $R_F = 20\ \Omega$  for  $G = +1$ ,  $R_F = 470\ \Omega$  for  $G = +2$ ,  $G = +10$ , and  $R_L = 150\ \Omega$ , unless otherwise noted.

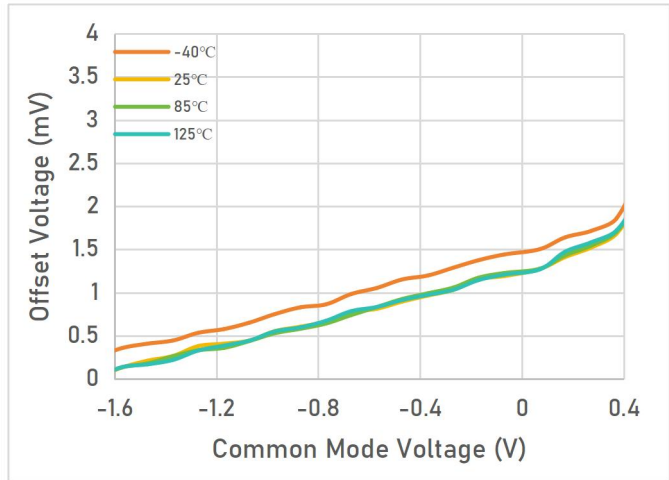
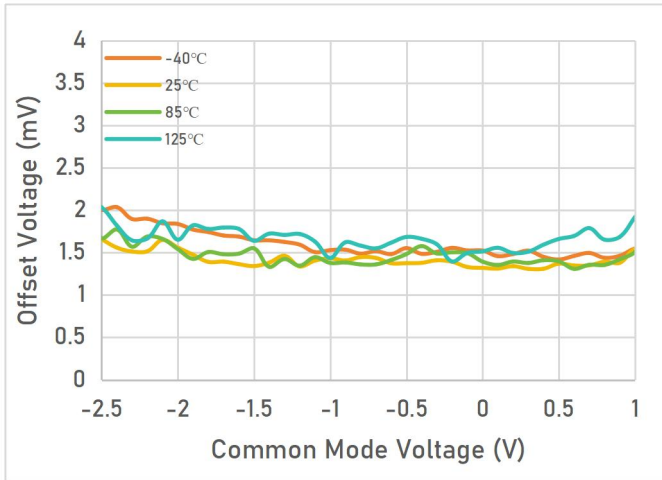


Figure 7. Offset Voltage vs Common Mode Voltage ( $V_S = \pm 2.5\text{ V}$ )

Figure 8. Offset Voltage vs Common Mode Voltage ( $V_S = \pm 1.65\text{ V}$ )

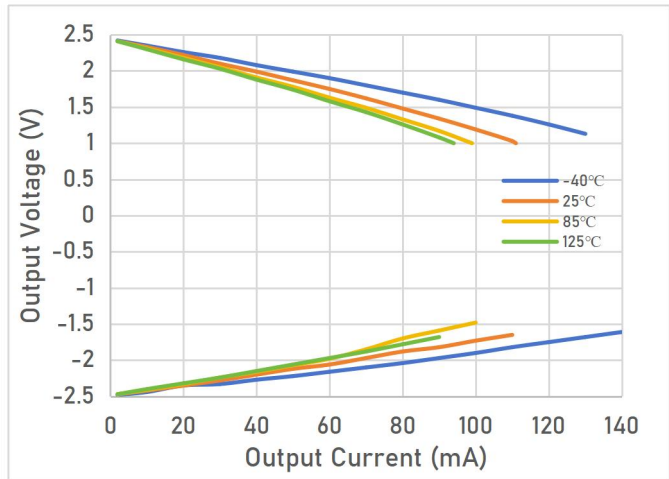
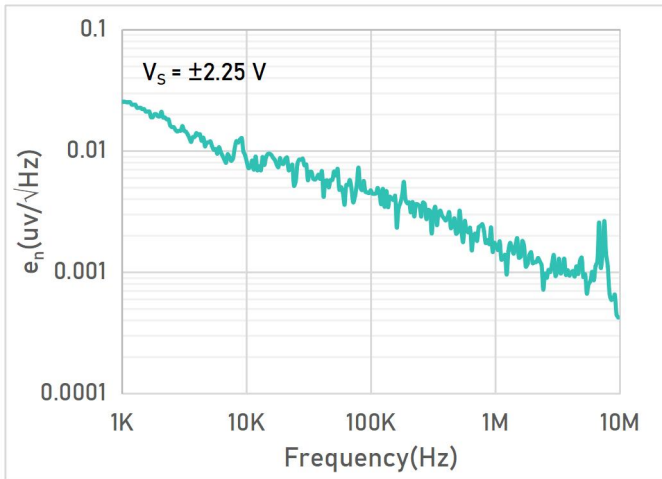


Figure 9. Input Voltage Noise vs Frequency

Figure 10. Output Voltage vs Output Current ( $V_S = \pm 2.5\text{ V}$ )

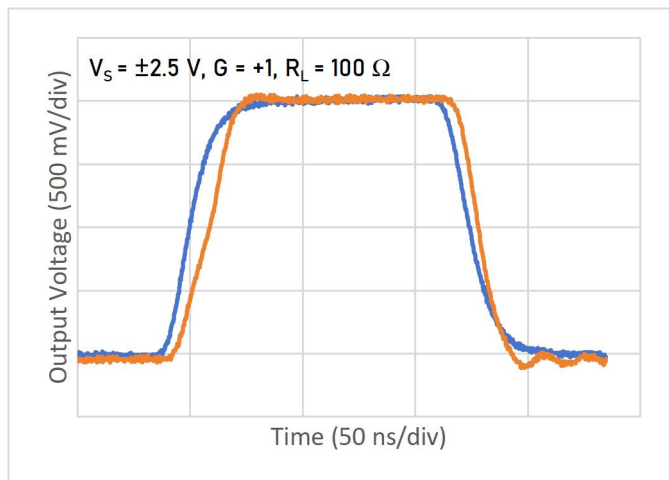
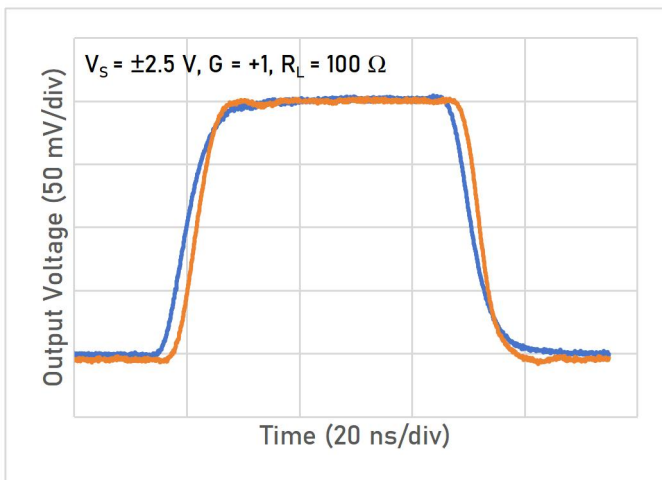


Figure 11. Non-Inverting Small-Signal Step Response

Figure 12. Non-Inverting Large-Signal Step Response

Typical Characteristics (cont.)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $R_F = 20\ \Omega$  for  $G = +1$ ,  $R_F = 470\ \Omega$  for  $G = +2$ ,  $G = +10$ , and  $R_L = 150\ \Omega$ , unless otherwise noted.

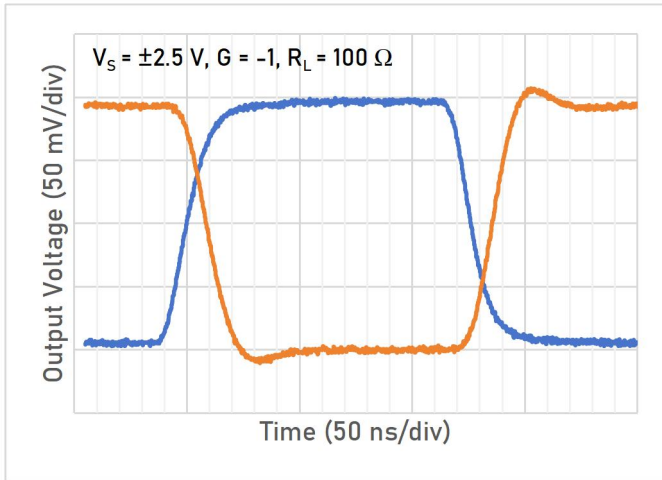


Figure 13. Inverting Small-Signal Step Response

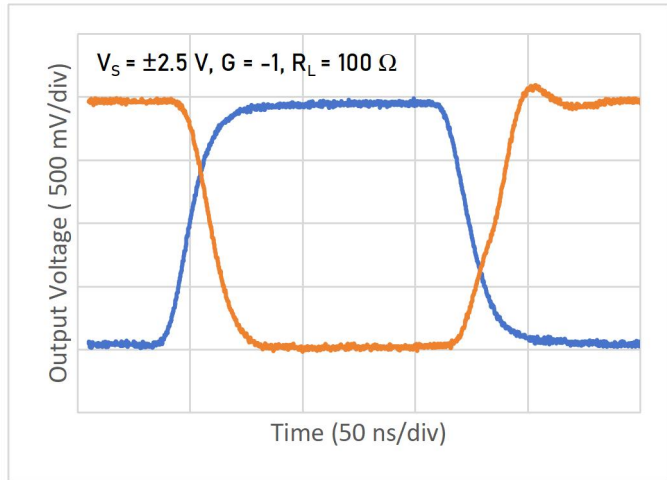


Figure 14. Inverting Large-Signal Step Response

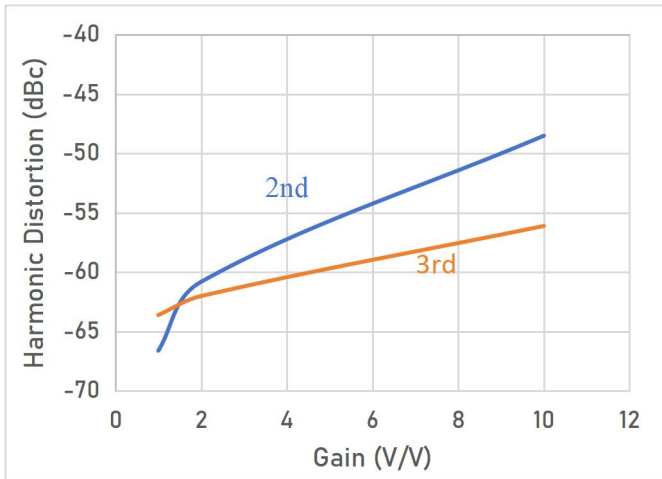


Figure 15. Harmonic Distortion vs Gain  
 $V_S = \pm 2.5\text{ V}$ ,  $f = 1\text{ MHz}$ ,  $V_o = 2V_{pp}$

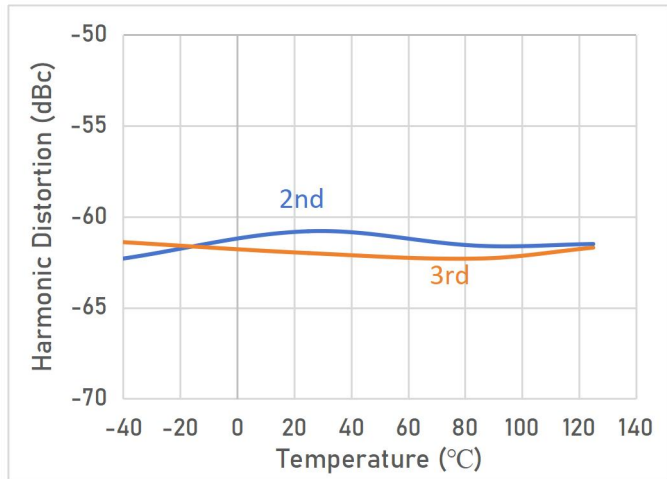


Figure 16. Harmonic Distortion vs Temperature  
 $V_S = \pm 2.5\text{ V}$ ,  $f = 1\text{ MHz}$ ,  $V_o = 2V_{pp}$

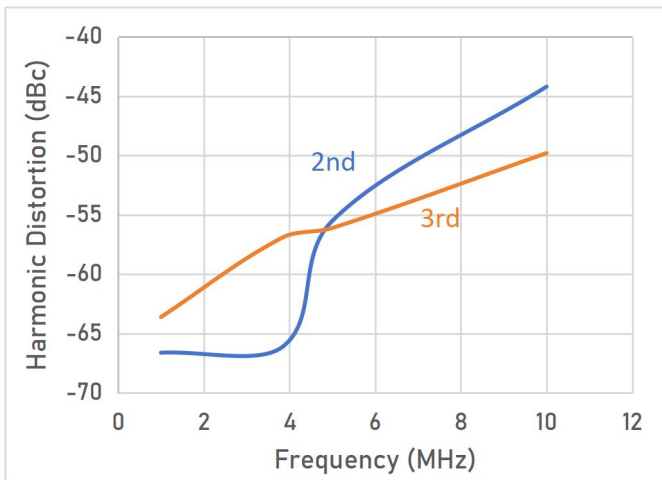


Figure 17. Harmonic Distortion vs Frequency  
 $V_S = \pm 2.5\text{ V}$ ,  $G = +1$ ,  $V_o = 2V_{pp}$

## Detailed Description

The LTA805x is a family of High speed, high slew rate, rail-to-rail output operational amplifiers specifically designed for high-speed applications. These devices operate from 3.3 V to 6.6 V at the temperature range of  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ , are unity-gain stable, and suitable for a wide range of general-purpose applications. The output stage is capable of driving heavy loads with 130 mA linear output current. The input common-mode voltage range includes from  $V_{S-} - 0.1\text{ V}$  to  $V_{S+} - 1\text{ V}$ , and allows the LTA805x family to be used in virtually any single supply application. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The LTA805x features 200 MHz bandwidth and 160 V/ $\mu\text{s}$  slew rate, providing good ac performance at same time. DC applications are also well served with low input bias current, and an input offset voltage of  $\pm 1.8\text{ mV}$  typically. The typical offset voltage drift is  $4\text{ }\mu\text{V}/^{\circ}\text{C}$ , over the full temperature range the input offset voltage changes only 660  $\mu\text{V}$ .

## Operating Voltage

The LTA805x family is optimized for operation at voltages as low as +3.3 V ( $\pm 1.65\text{ V}$ ) and up to +6.6 V ( $\pm 3.3\text{ V}$ ). In addition, many specifications apply from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ . Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

## Rail to rail output

Designed as a high speed, high slew rate, low-noise operational amplifier, the LTA805x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 100  $\Omega$ , the output swings typically to within 350-mV of 5 V supply rail. Different load conditions change the ability of the amplifier to swing close to the rails. For in open load, the output swings typically to within 40 mV of the positive supply rail and within 5 mV of the negative supply rail.

## Capacitive load and stability

As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to overshooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the LTA805x op-amps must drive a heavy capacitive load. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor,  $R_{IS0}$ , between the amplifier output terminal and the load capacitance, as shown in Figure 1.  $R_{IS0}$  isolates the amplifier output and feedback network from the capacitive load. The bigger the  $R_{IS0}$  resistor value, the more stable  $V_{OUT}$  will be. Note that this method results in a loss of gain accuracy because  $R_{IS0}$  forms a voltage divider with the  $R_L$ .

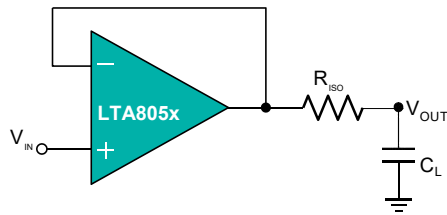


Figure 1. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 2. It provides DC accuracy as well as AC stability. The  $R_F$  provides the DC accuracy by connecting the inverting signal with the output.

The  $C_F$  and  $R_{ISO}$  serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two other ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

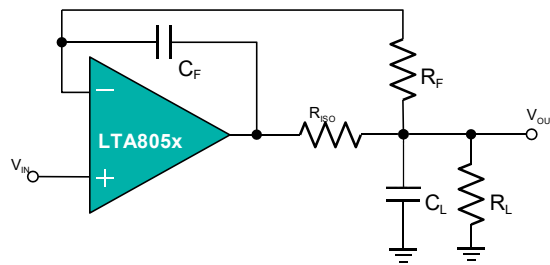


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

## Typical Application Circuit

### Active filter

The LTA805x family is well-suited for active filter applications that require a wide bandwidth, fast slew rate, single-supply operational amplifier. Figure 3 shows a 500 kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cut-off frequency, roll-off is  $-40$  dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

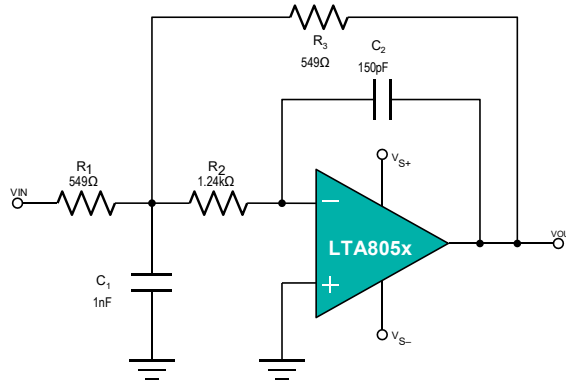


Figure 3. Second-Order, Butterworth, 500-kHz Low-Pass Filter

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a non-inverting output can be achieved through one of these options:

1. adding an inverting amplifier ;
2. adding an additional second-order MFB stage;
3. using a non-inverting filter topology, such as the Sallen-Key (shown in Figure 4).

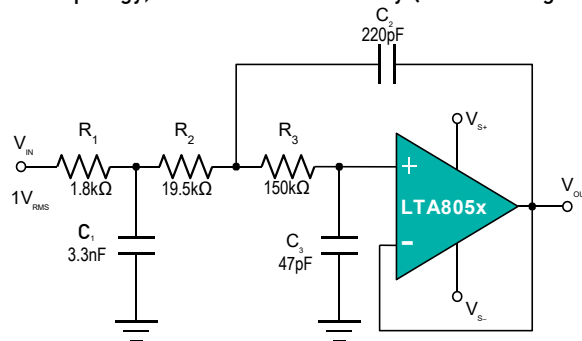


Figure 4. Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

### Differential amplifier

The circuit shown in Figure 5 performs the difference function. If the resistors ratios are equal  $R_4/R_3 = R_2/R_1$ , then:

$$V_{OUT} = (V_p - V_n) * R_2/R_1 + V_{REF}$$

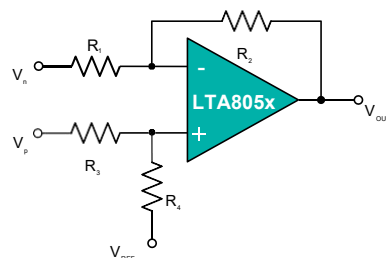
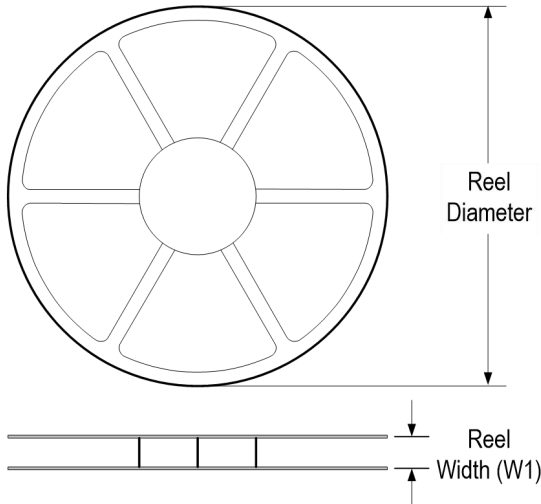


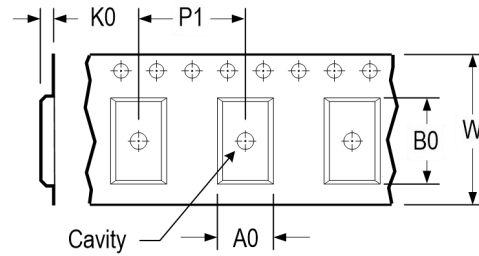
Figure 5. Differential Amplifier

Tape and Reel Information

REEL DIMENSIONS

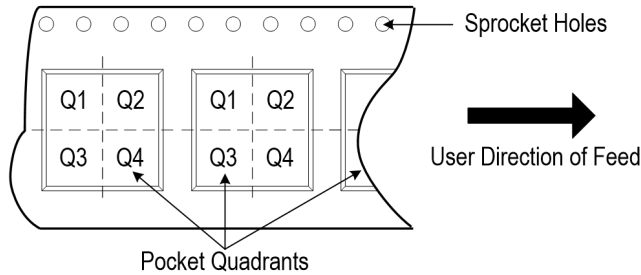


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

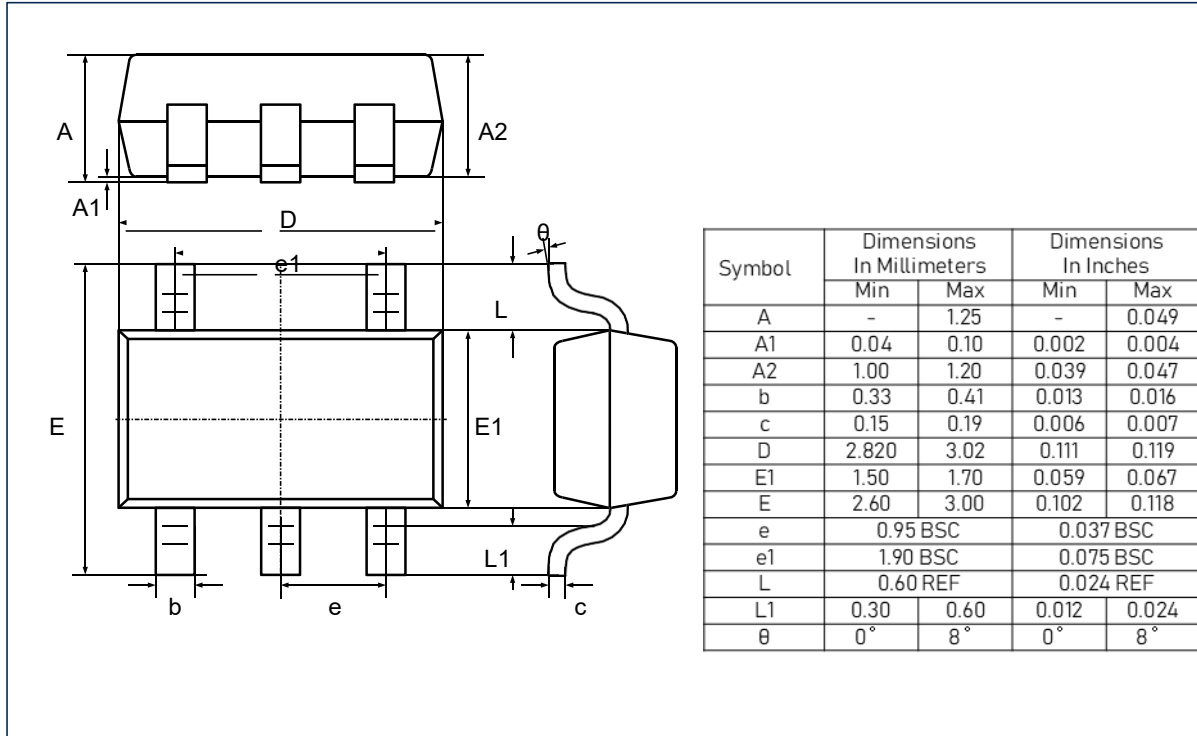


\* All dimensions are nominal

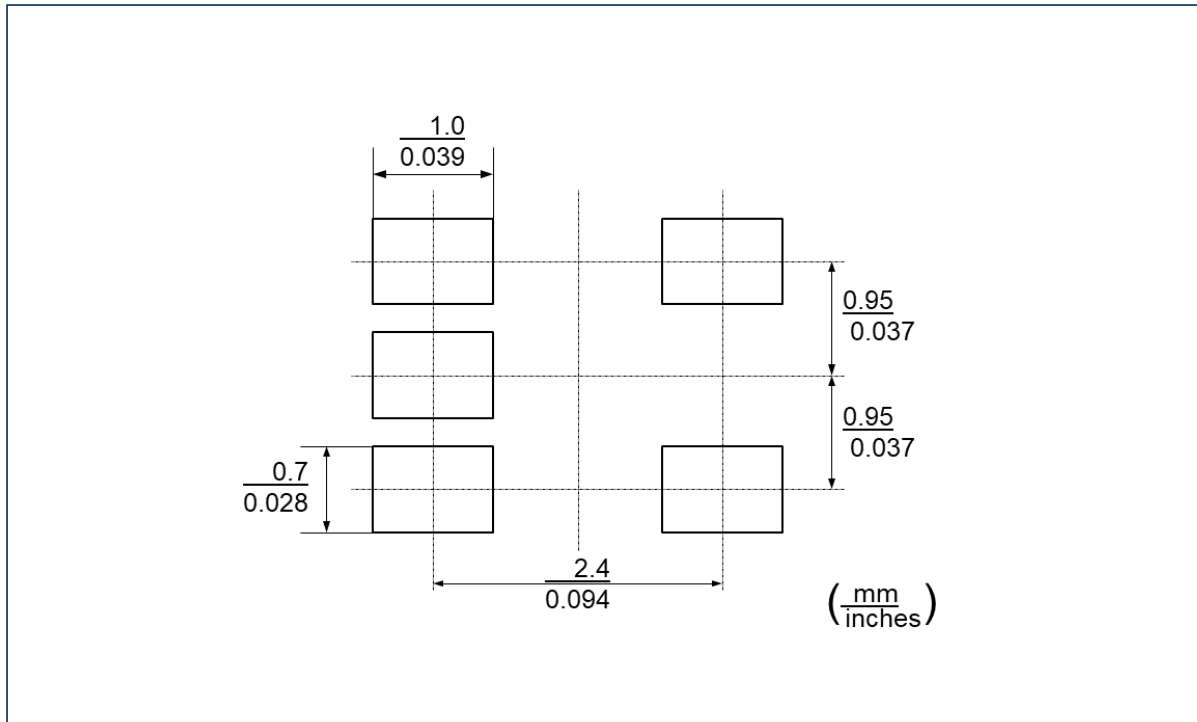
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA8051XT5/R6	SOT23	5	3 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTA8051XS8/R8	SOIC	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTA8052XS8/R8	SOIC	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTA8052XV8/R6	MSOP	8	3 000	330	12.5	5.0	3.5	2.0	8.0	12.0	Q1
LTA8054XS14/R5	SOIC	14	2 500	330	12.5	6.5	9.5	2.0	8.0	16.0	Q1
LTA8054XT14/R6	TSSOP	14	3 000	330	12.5	6.9	5.5	1.3	8.0	16.0	Q1

Package Outlines

DIMENSIONS, SOT23-5L

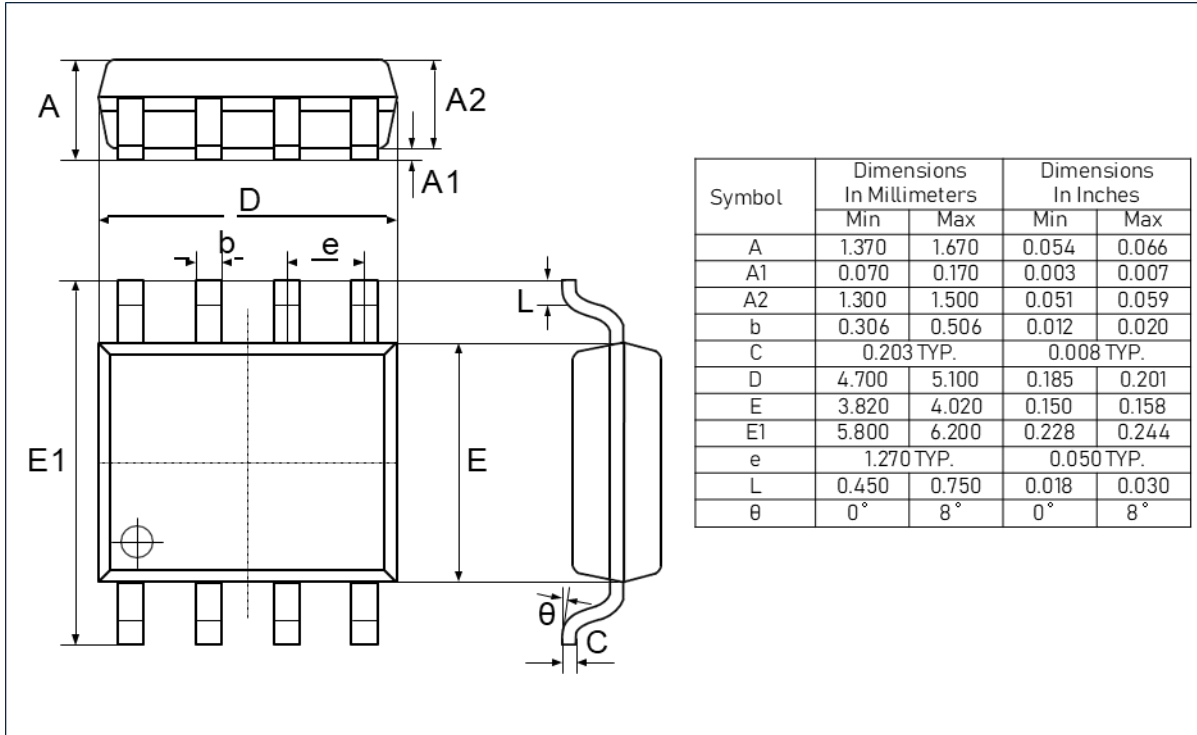


RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L

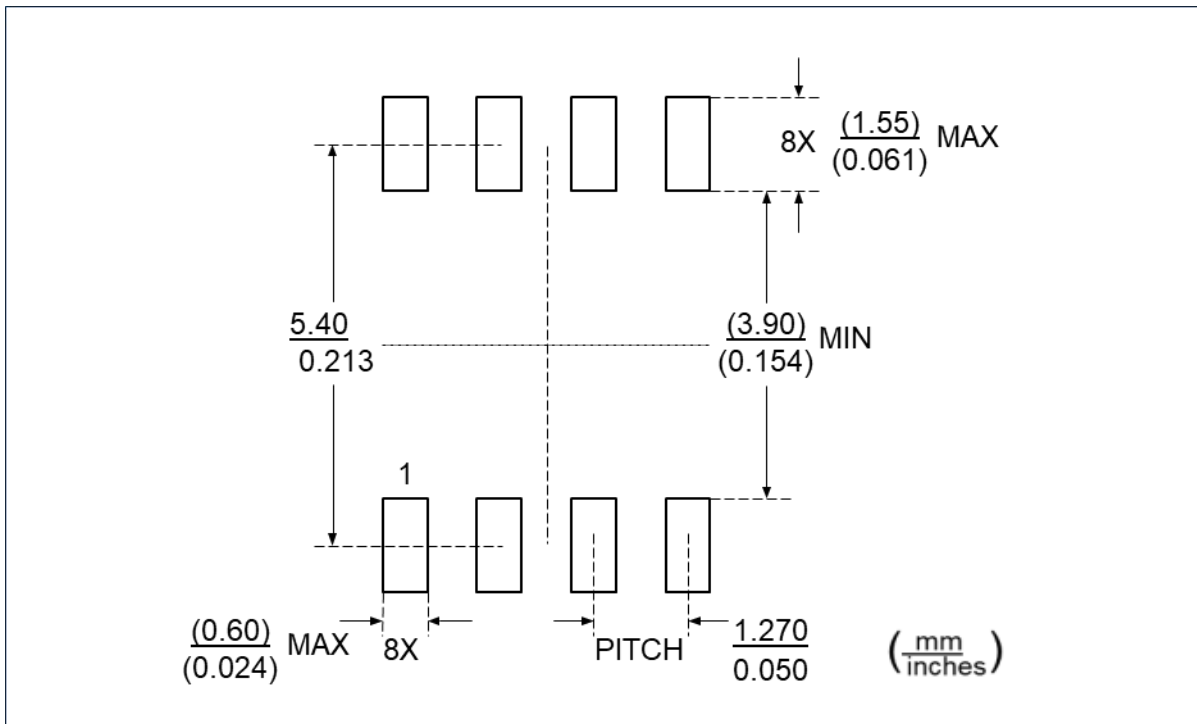


Package Outlines (cont.)

DIMENSIONS, SOIC-8L

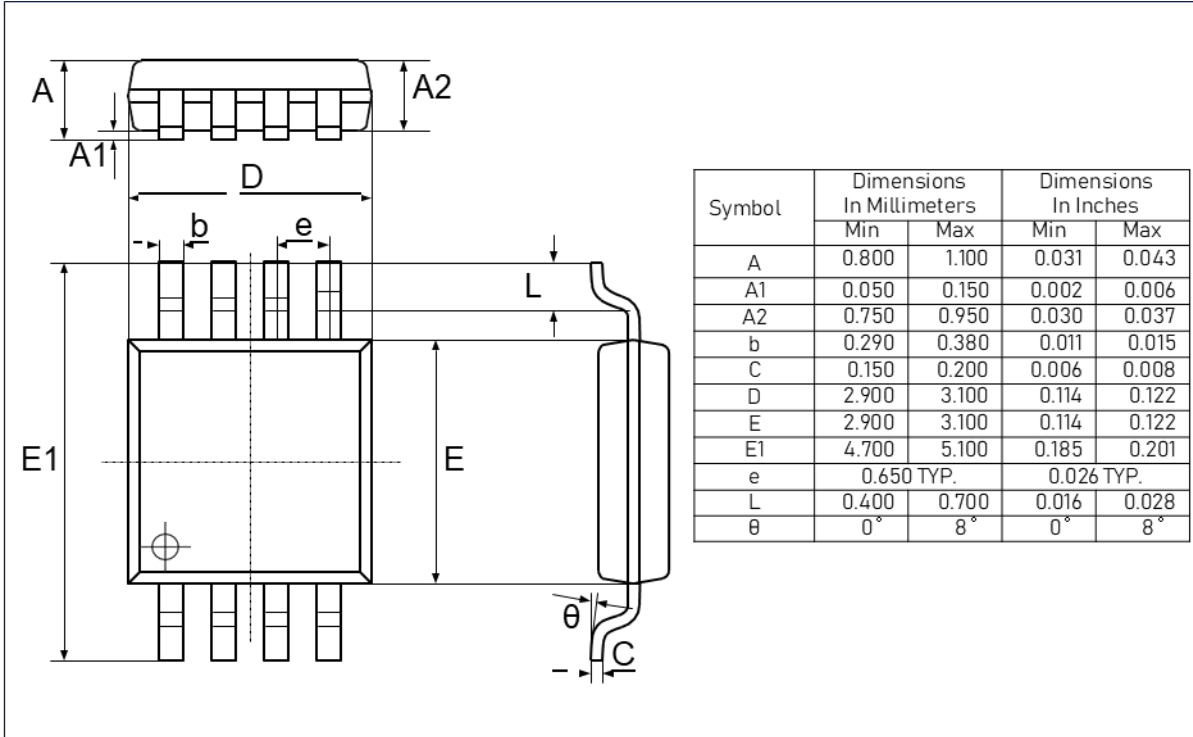


RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L

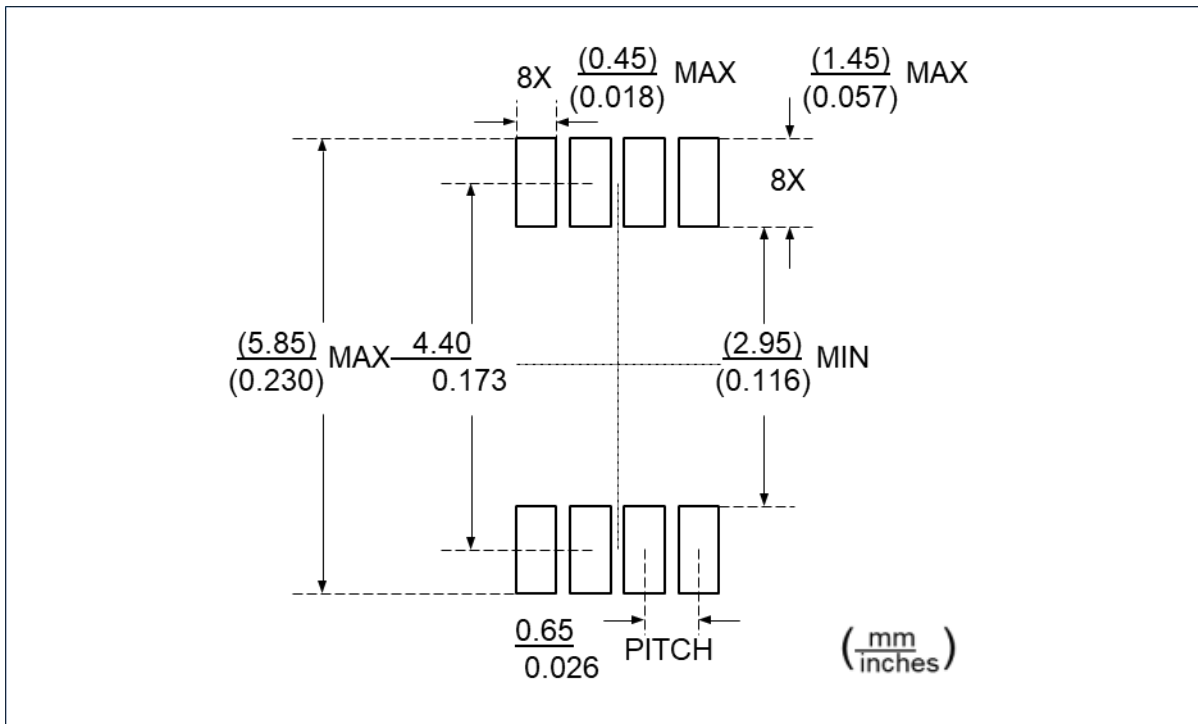


Package Outlines (cont.)

DIMENSIONS, MSOP-8L

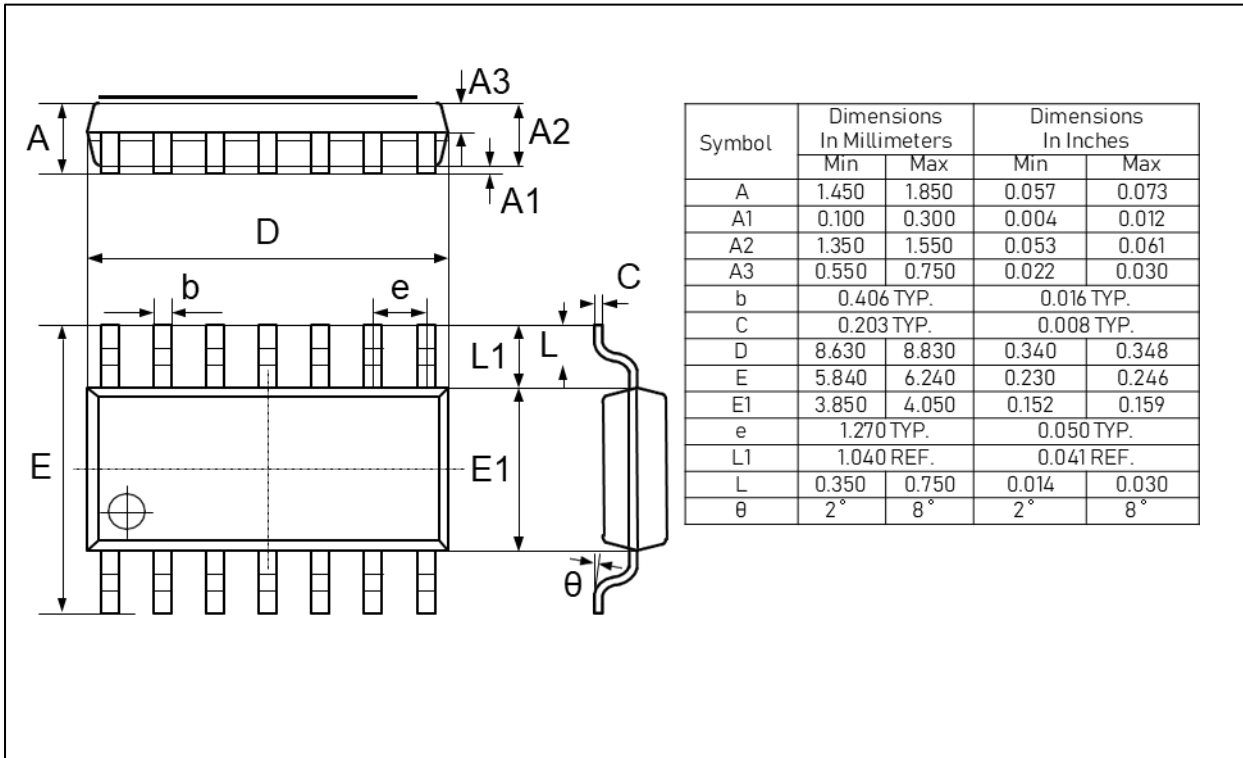


RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L

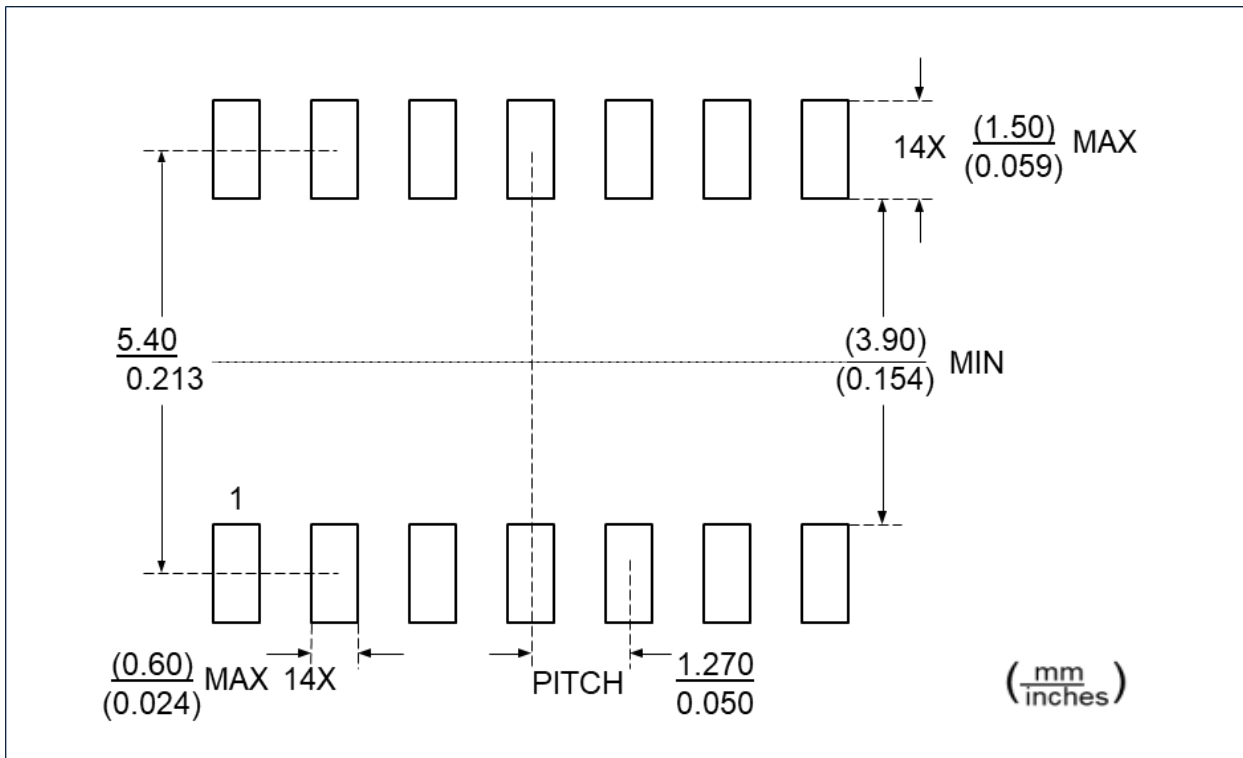


Package Outlines (cont.)

DIMENSIONS, SOIC-14L

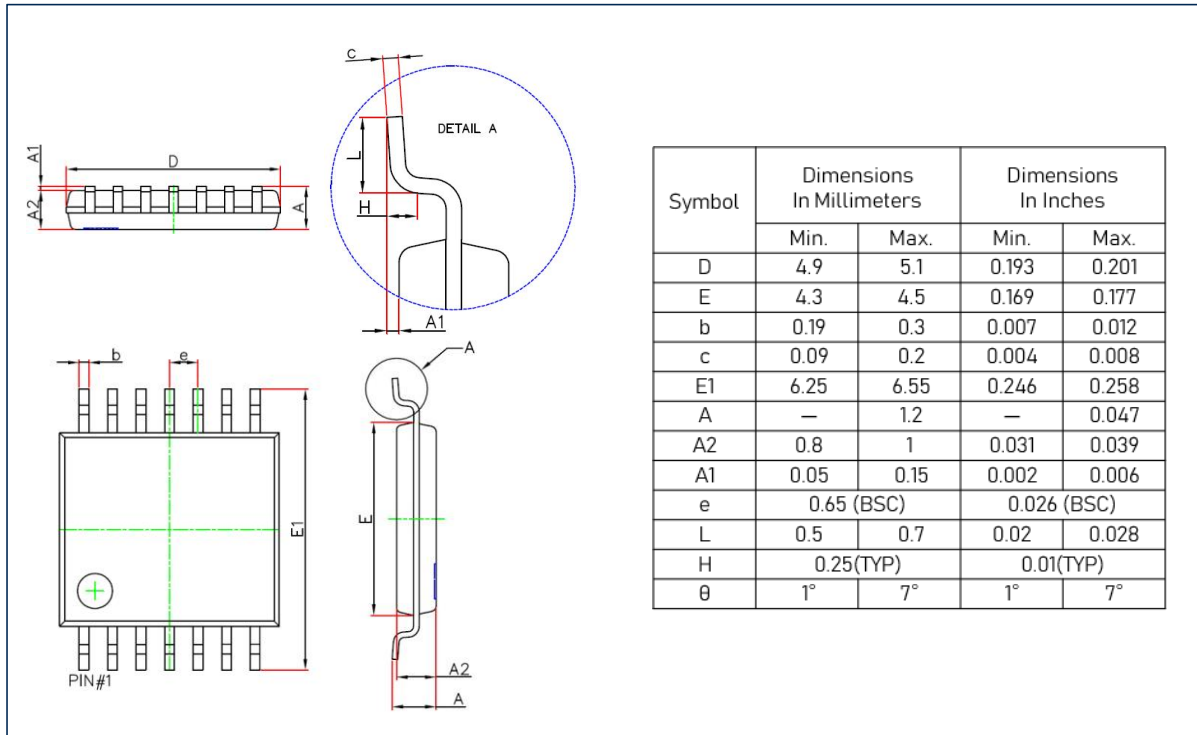


RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L

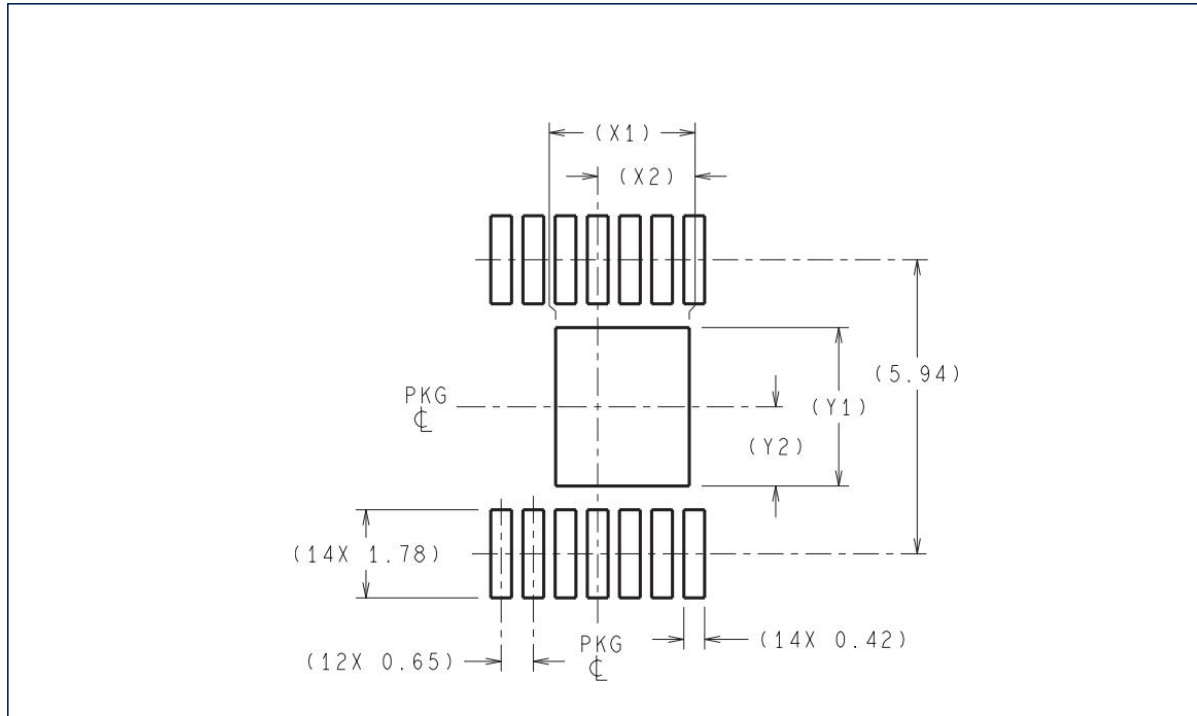


Package Outlines (cont.)

DIMENSIONS, TSSOP-14L



RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L



### Important Notice

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