

## General Description

The LTA8081E, LTA8082E and LTA8084E (LTA808xE) are a family of low power, 48 V wide supply voltage, rail-to-rail output, precision operational amplifiers capable of operating on supplies ranging from +4.5 V ( $\pm 2.25$  V) to +48 V ( $\pm 24$  V). This new generation of high-voltage CMOS operational amplifiers, in conjunction with the LTA809xE, provide a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications. The LTA808xE devices offer outstanding dc precision and ac performance, including low offset ( $\pm 75$   $\mu$ V typically), low offset drift ( $\pm 1.5$   $\mu$ V/ $^{\circ}$ C typically), 10 MHz bandwidth, and 8 nV/ $\sqrt{\text{Hz}}$  input voltage noise density at 10 kHz. Unique features such as differential input-voltage range to the negative supply rail, high output current ( $\pm 45$  mA), high capacitive load drive of up to 1 nF, and high slew rate (6 V/ $\mu$ s) make the LTA808xE high-performance operational amplifiers for high-voltage industrial applications.

The robust design of the LTA808xE family provides ease-of-use to the circuit designer: integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection. The LTA808xE are optimized for operation at voltages from +4.5 V ( $\pm 2.25$  V) to +48V ( $\pm 24$  V) over the extended temperature range of  $-40$   $^{\circ}$ C to +125  $^{\circ}$ C.

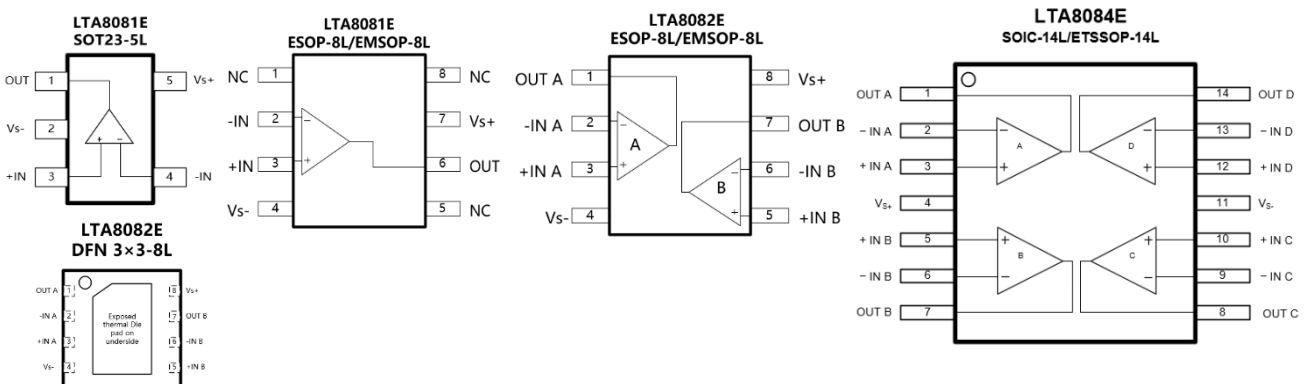
## Features and Benefits

- Wide Supply:  $\pm 2.25$  V to  $\pm 24$  V, 4.5 V to 48 V
- Low Offset Voltage:  $\pm 75$   $\mu$ V Typically
- Low Offset Voltage Drift:  $\pm 1.5$   $\mu$ V/ $^{\circ}$ C
- High Common-Mode Rejection: 113 dB
- Gain Bandwidth: 10 MHz
- Slew Rate: 6 V/ $\mu$ s
- Low Noise: 8 nV/ $\sqrt{\text{Hz}}$  at 10 kHz
- Low Bias Current:  $\pm 10$  pA
- Rail-to-Rail Output

## Applications

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- High-Side and Low-Side Current Sensing
- High Precision Comparator
- Battery-Powered Instruments
- Test and Measurement Equipment
- Multiplexed Data-Acquisition Systems
- Programmable Logic Controllers

## Pin Configuration (Top View)



## Pin Description

Symbol	Description
-IN	Inverting input of the amplifier. The voltage range is from $V_{S-}$ to $V_{S+} - 1.5$ V.
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as -IN.
$V_{S+}$	Positive power supply. The voltage is from 4.5 V to 48 V. Split supplies are possible as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 4.5 V to 48 V.
$V_{S-}$	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 4.5 V to 48 V.
OUT	Amplifier output.
NC	No connection.

## Ordering Information

Type Number	Package Name	Package Quantity	Eco Class	Marking Code
LTA8081EXT5/R6	SOT23-5L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	H81
LTA8081EXS8/R8	ESOP-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	HV81E
LTA8081EXV8/R6	EMSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	HV81E
LTA8082EXS8/R8	ESOP-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	HV82E
LTA8082EXV8/R6	EMSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	HV82E
LTA8082EXF8/R10	DFN3x3-8L	Tape and Reel, 5 000	Green (RoHS & no Sb/Br)	HV82E
LTA8084EXS14/R5	SOIC-14L	Tape and Reel, 2 500	Green (RoHS & no Sb/Br)	HV84E
LTA8084EXT14/R6	ETSSOP-14L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	HV84E

## Limiting Value- In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, $V_{S+}$ to $V_{S-}$	60 V
Signal Input Terminals: Voltage, Current	$V_{S-} - 0.3$ V to $V_{S+} + 0.3$ V, $\pm 10$ mA
Output Short-Circuit	Continuous
Storage Temperature Range, $T_{stg}$	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Junction Temperature, $T_J$	150 $^{\circ}\text{C}$
Lead Temperature Range (Soldering 10 sec)	260 $^{\circ}\text{C}$

## ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	2 000	V
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	2 000	

## Electrical Characteristics

$V_S = 4.5 \text{ V to } 48 \text{ V}$ ,  $T_A = +25 \text{ }^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10 \text{ k}\Omega$  connected to  $V_S / 2$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>OFFSET VOLTAGE</b>						
Input Offset Voltage	$V_{OS}$	$V_S = 48 \text{ V}$		$\pm 75$	$\pm 350$	$\mu\text{V}$
Offset voltage drift	$V_{OS \text{ TC}}$	$T_A = -40 \text{ to } +125^\circ\text{C}$		$\pm 1.5$		$\mu\text{V}/^\circ\text{C}$
Power supply rejection ratio	PSRR	$V_S = 4.5 \text{ to } 48 \text{ V}$ , $V_{CM} = 0.1 \text{ V}$	91	118		dB
		$T_A = -40 \text{ to } +125^\circ\text{C}$		90		
<b>INPUT BIAS CURRENT</b>						
Input bias current	$I_B$			10		pA
		$T_A = -40 \text{ to } +85^\circ\text{C}$		150		
		$T_A = -40 \text{ to } +125^\circ\text{C}$		600		
Input offset current	$I_{OS}$			5		pA
<b>POWER SUPPLY</b>						
Quiescent current (per amplifier)	$I_Q$	$V_S = 4.5 \text{ V}$		2.1		mA
		$V_S = 48 \text{ V}$		3.1		
<b>NOISE</b>						
Input voltage noise	$V_n$	$f = 0.1 \text{ to } 10 \text{ Hz}$		4		$\mu\text{V}_{P-P}$
Input current noise density	$I_n$	$f = 1 \text{ kHz}$		5		$\text{fA}/\sqrt{\text{Hz}}$
Input voltage noise density	$e_n$	$f = 1 \text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10 \text{ kHz}$		8		
<b>INPUT VOLTAGE</b>						
Common-mode voltage range	$V_{CM}$		$V_{S-}$		$V_{S+} - 1.5$	V
Common-mode rejection ratio	CMRR	$V_S = 48 \text{ V}$ , $V_{CM} = 0 \text{ to } 46 \text{ V}$	86	113		dB
		$V_{CM} = 0.1 \text{ to } 38 \text{ V}$ , $T_A = -40 \text{ to } +125^\circ\text{C}$		103		
		$V_S = 4.5 \text{ V}$ , $V_{CM} = 0 \text{ to } 2.5 \text{ V}$	66	93		
		$V_{CM} = 0.1 \text{ to } 2 \text{ V}$ , $T_A = -40 \text{ to } +125^\circ\text{C}$		84		
<b>INPUT IMPEDANCE</b>						
Input capacitance	$C_{IN}$	Differential		2		pF
		Common mode		3.5		
<b>OPEN-LOOP GAIN</b>						
Open-loop voltage gain	$A_{VOL}$	$V_S = 48 \text{ V}$ , $V_O = 0.1 \text{ to } 39.9 \text{ V}$	115	120		dB
		$T_A = -40 \text{ to } +125^\circ\text{C}$		110		
		$V_S = 4.5 \text{ V}$ , $V_O = 0.1 \text{ to } 4.4 \text{ V}$	100	115		
		$T_A = -40 \text{ to } +125^\circ\text{C}$		100		

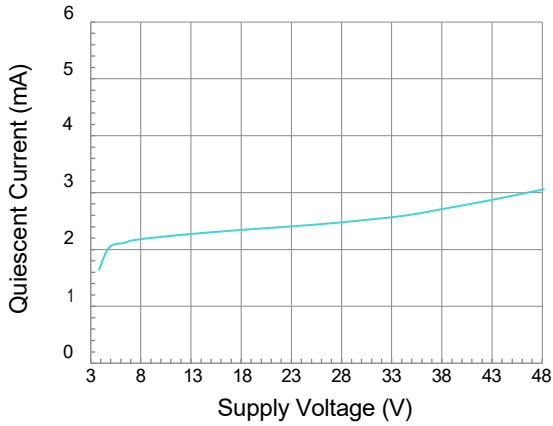
## Electrical Characteristics (Cont.)

$V_S = 4.5 \text{ V to } 48 \text{ V}$ ,  $T_A = +25 \text{ }^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10 \text{ k}\Omega$  connected to  $V_S / 2$ , unless otherwise noted.

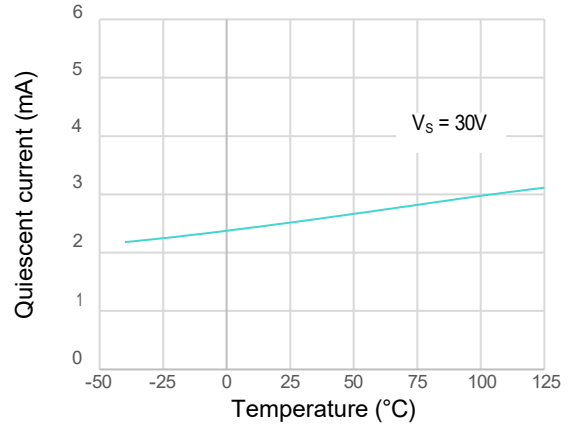
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>FREQUENCY RESPONSE</b>						
Gain bandwidth product	GBW			10		MHz
Slew rate	SR	$V_S = 30 \text{ V}$ , $G = +1$ , 8 V step		6		V/ $\mu$ s
Total harmonic distortion + noise	THD+N	$G = +1$ , $f = 1 \text{ kHz}$ , $V_O = 3 V_{RMS}$		0.0002		%
Settling time	$t_s$	To 0.1%, $V_S = 40 \text{ V}$ , $G = +1$ , 5 V step		2		$\mu$ s
		To 0.01%, $V_S = 40 \text{ V}$ , $G = +1$ , 5 V step		3.5		
Overload recovery time	$t_{OR}$	$V_{IN} \times \text{Gain} > V_S$		0.6		$\mu$ s
<b>THERMAL CHARACTERISTICS</b>						
Operating temperature range	$T_A$		-40		125	$^\circ\text{C}$
Package Thermal Resistance	$\theta_{JA}$	SOT23-5L		190		$^\circ\text{C/W}$
		ESOP-8L		50		
		EMSOP-8L		60		
		DFN3x3-8L		94		
		SOIC-14L		115		
		ETSSOP-14L		55		

### Typical Performance Characteristics

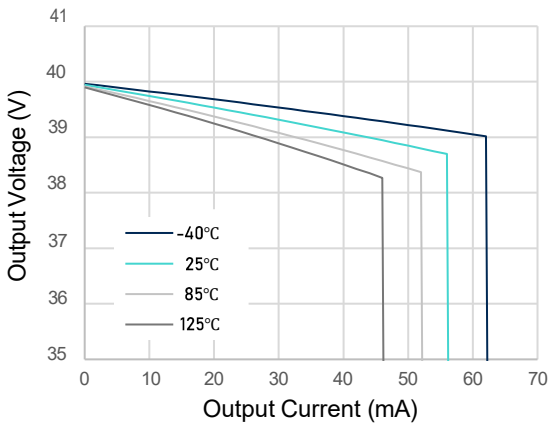
At  $T_A = +25^\circ\text{C}$ ,  $V_{CM} = V_S/2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



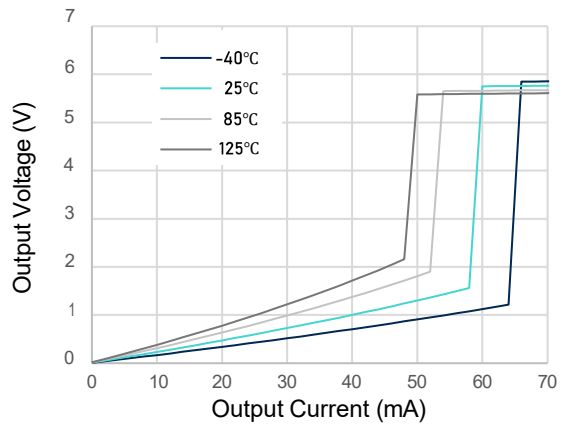
Quiescent Current as a function of Supply Voltage



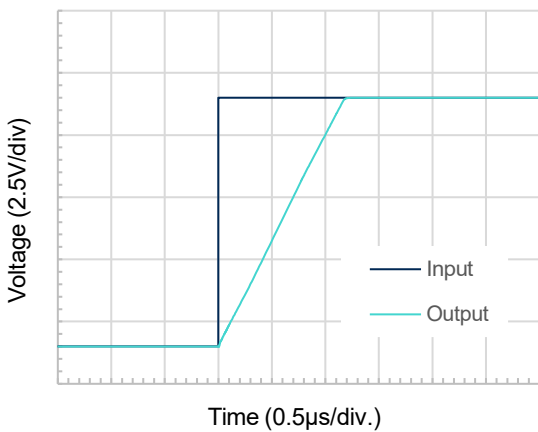
Quiescent Current as a function of Temperature



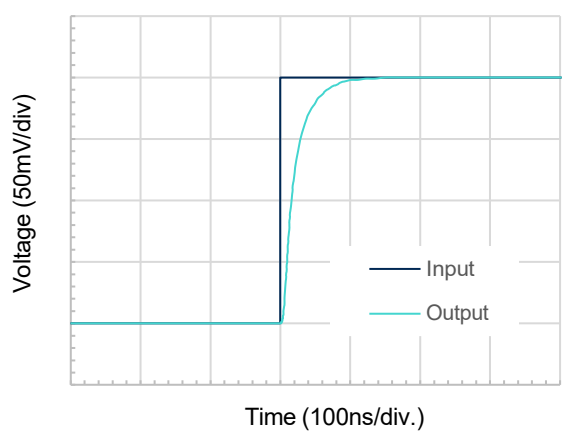
Output Voltage Swing as a function of Output Current (Sourcing,  $V_S = 40\text{ V}$ )



Output Voltage Swing as a function of Output Current (Sinking,  $V_S = 40\text{ V}$ )



Large-Signal Step Response (Rising)

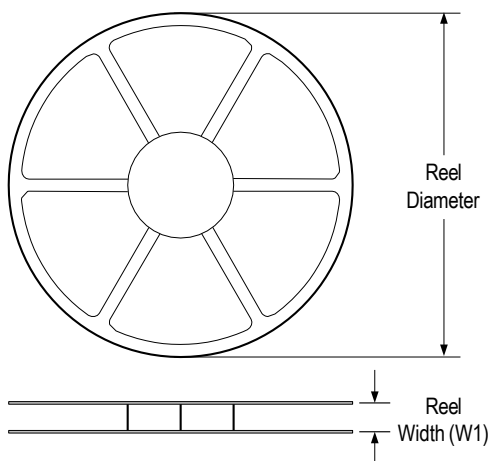


Small-Signal Step Response (Rising)

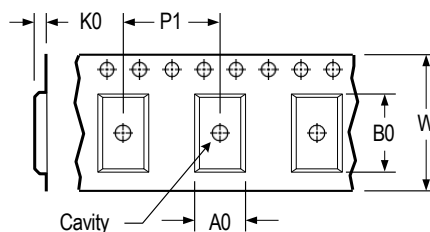
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Tape and Reel Information

REEL DIMENSIONS

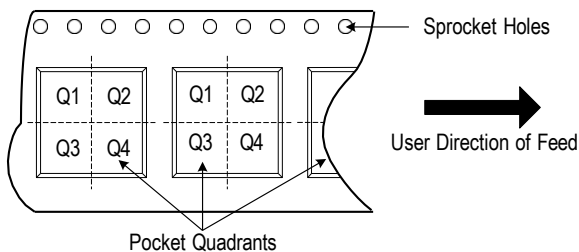


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

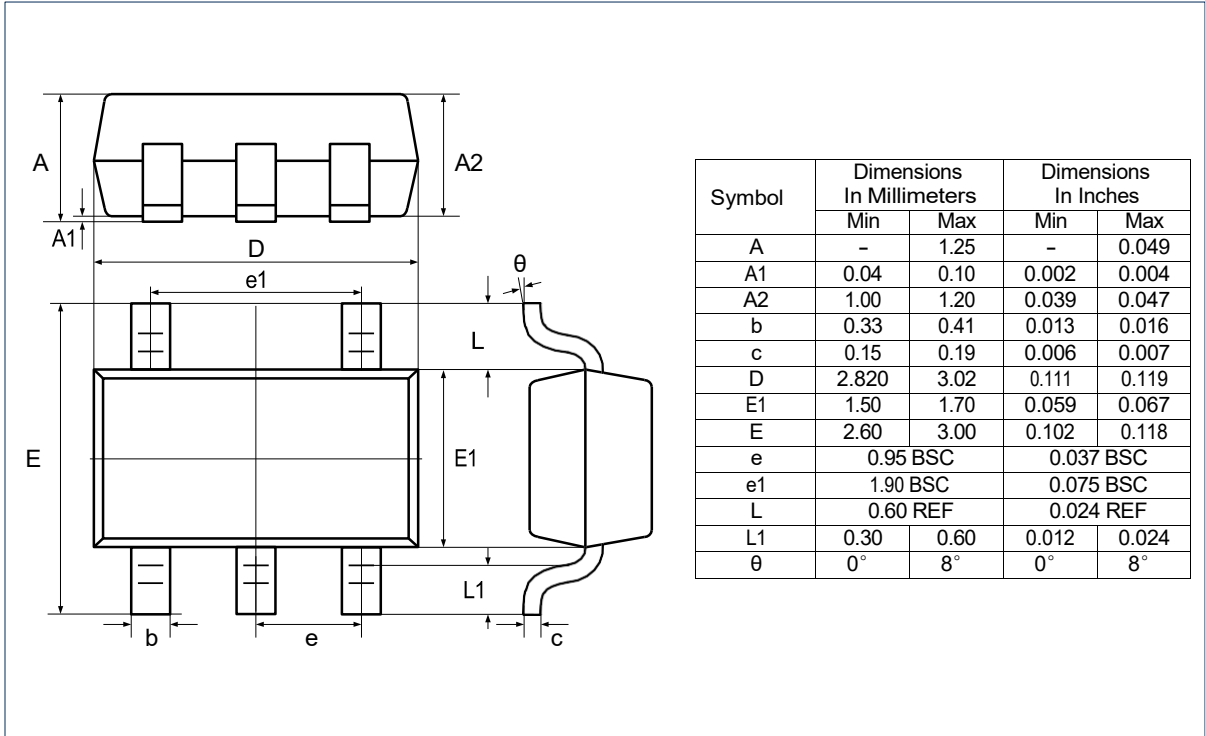


\* All dimensions are nominal.

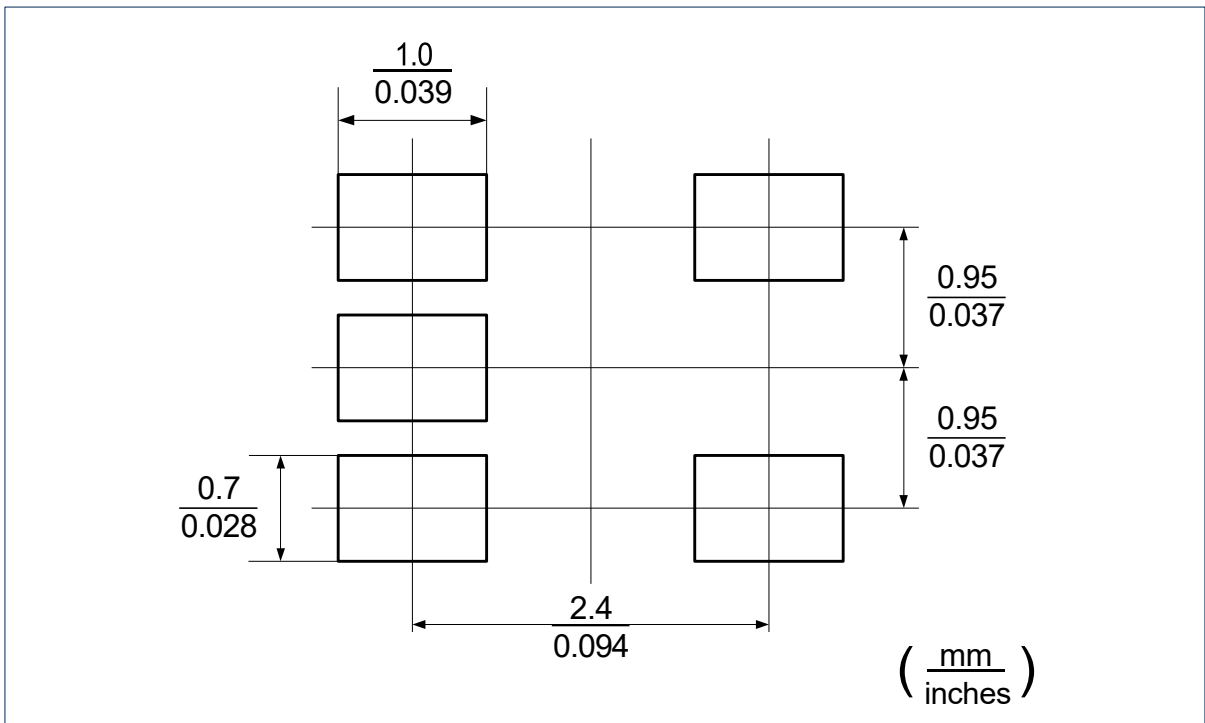
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA8081EXT5/R6	SOT23	5	3 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTA8081EXS8/R8	ESOP	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTA8081EXV8/R6	EMSOP	8	3 000	330	12.5	5.0	3.5	2.0	8.0	12.0	Q1
LTA8082EXS8/R8	ESOP	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTA8082EXV8/R6	EMSOP	8	3 000	330	12.5	5.0	3.5	2.0	8.0	12.0	Q1
LTA8082EXF8/R10	DFN3*3	8	5 000	330	12.5	3.3	3.3	1.1	8.0	12.0	Q1
LTA8084EXS14/R5	SOIC	14	2 500	330	12.5	6.5	9.5	2.0	8.0	16.0	Q1
LTA8084EXT14/R6	ETSSOP	14	3 000	330	12.5	6.9	5.5	1.3	8.0	16.0	Q1

Package Outlines

DIMENSIONS, SOT23-5L

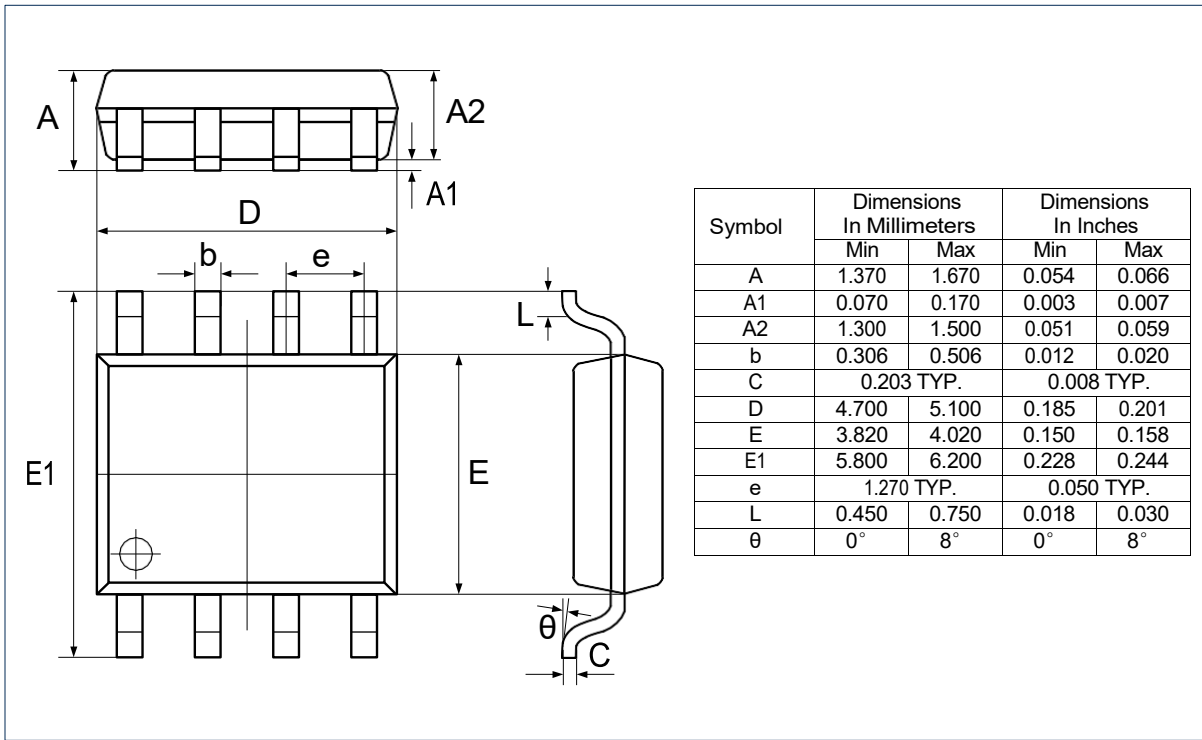


RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L

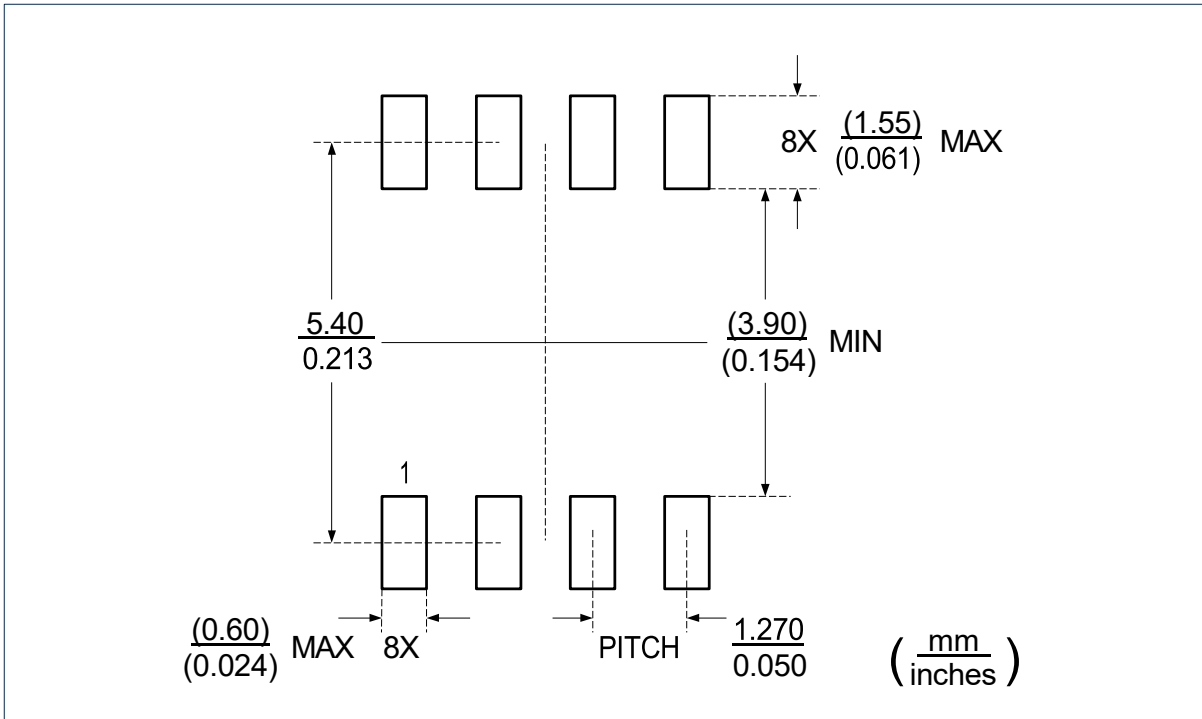


Package Outlines (continued)

DIMENSIONS, ESOP-8L

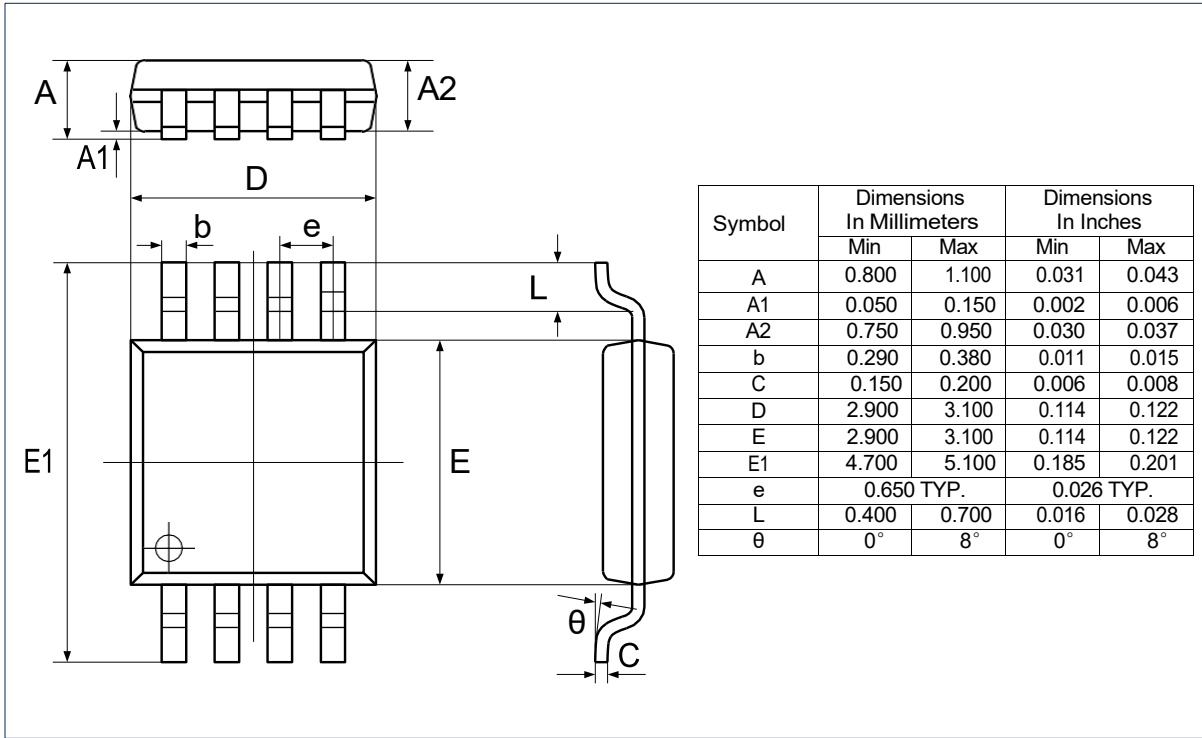


RECOMMENDED SOLDERING FOOTPRINT, ESOP-8L

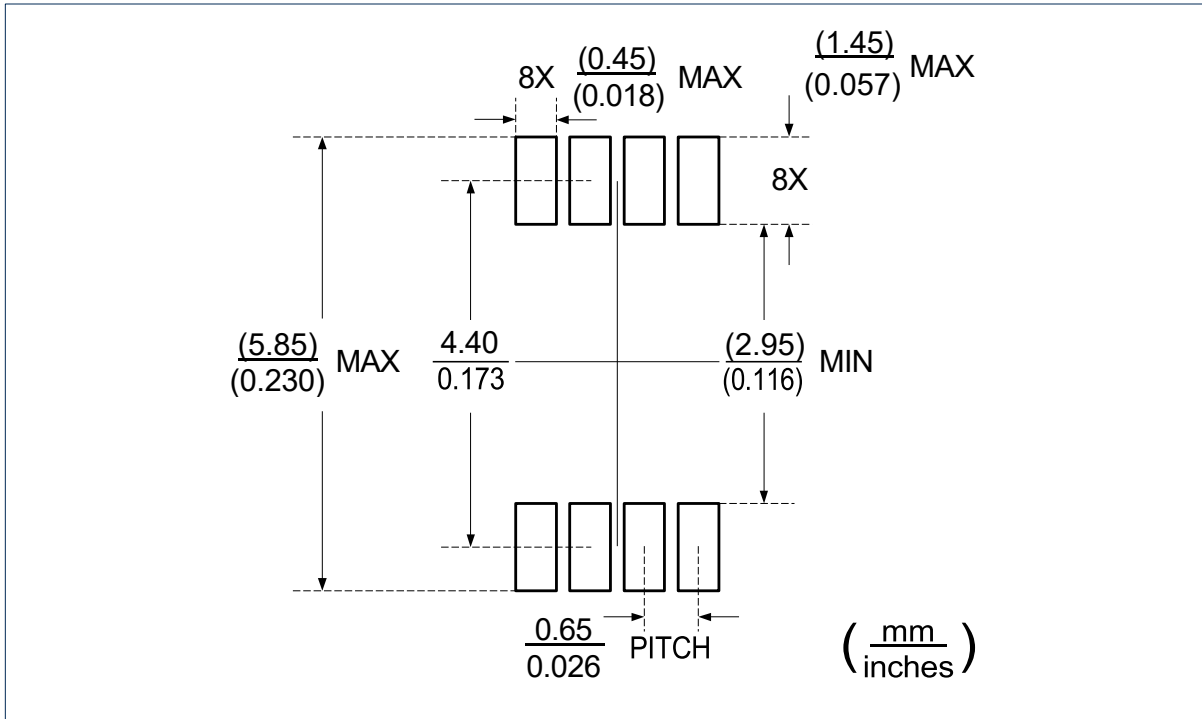


Package Outlines (continued)

DIMENSIONS, EMSOP-8L



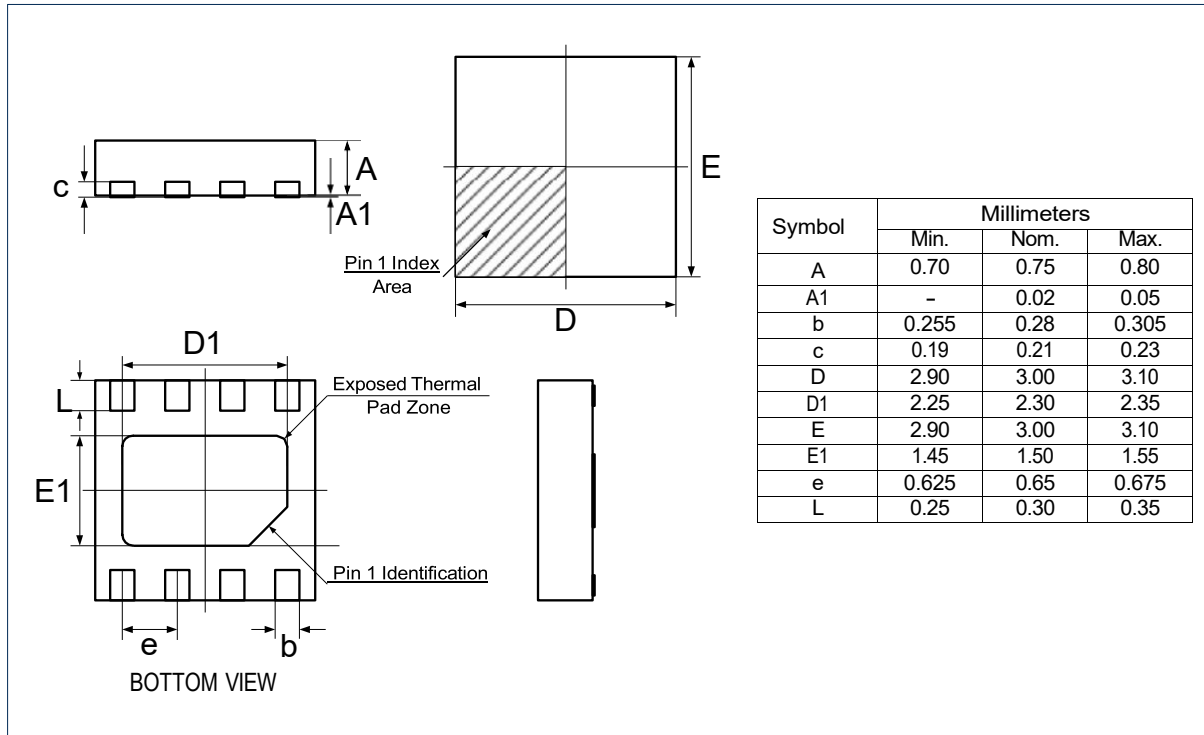
RECOMMENDED SOLDERING FOOTPRINT, EMSOP-8L



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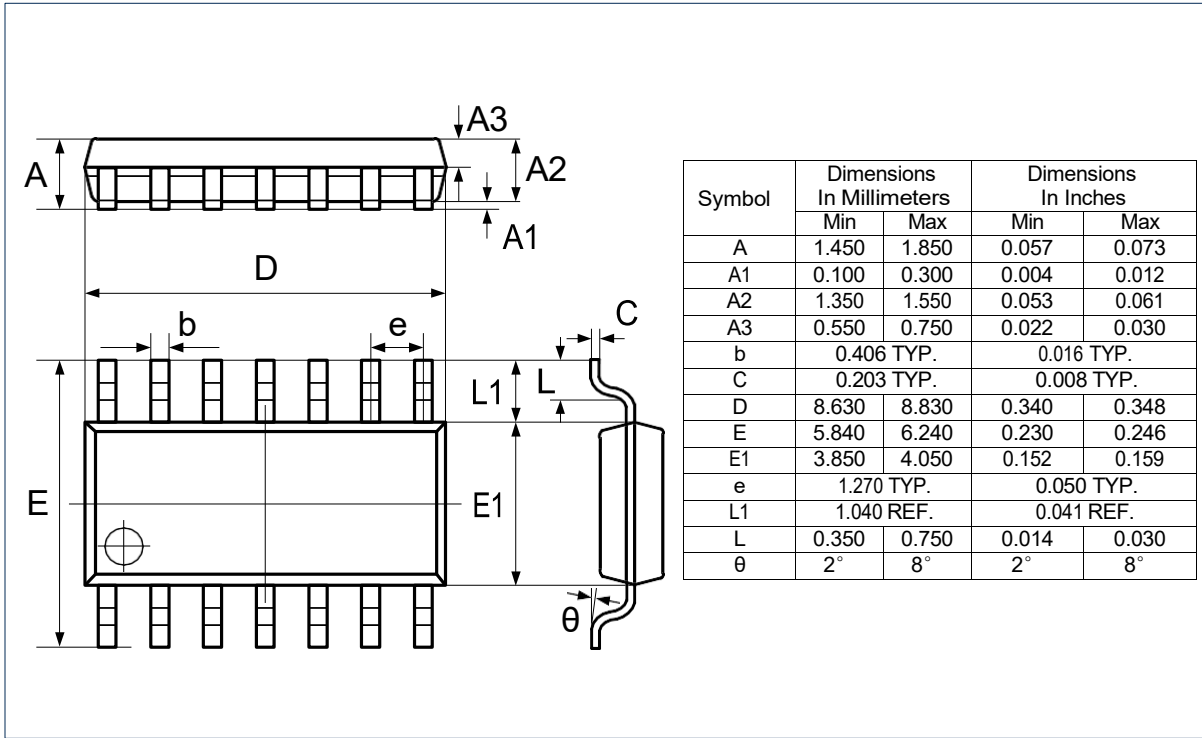
## Package Outlines (continued)

DIMENSIONS, DFN3x3-8L

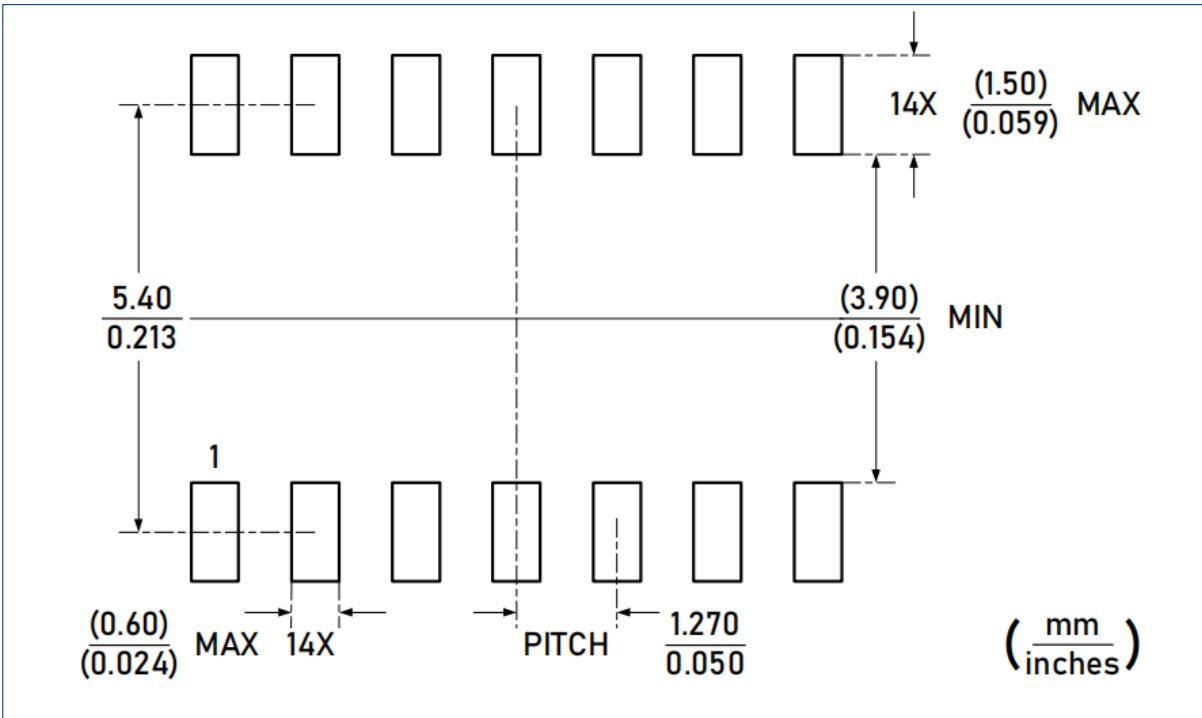


Package Outlines (continued)

DIMENSIONS, SOIC-14L



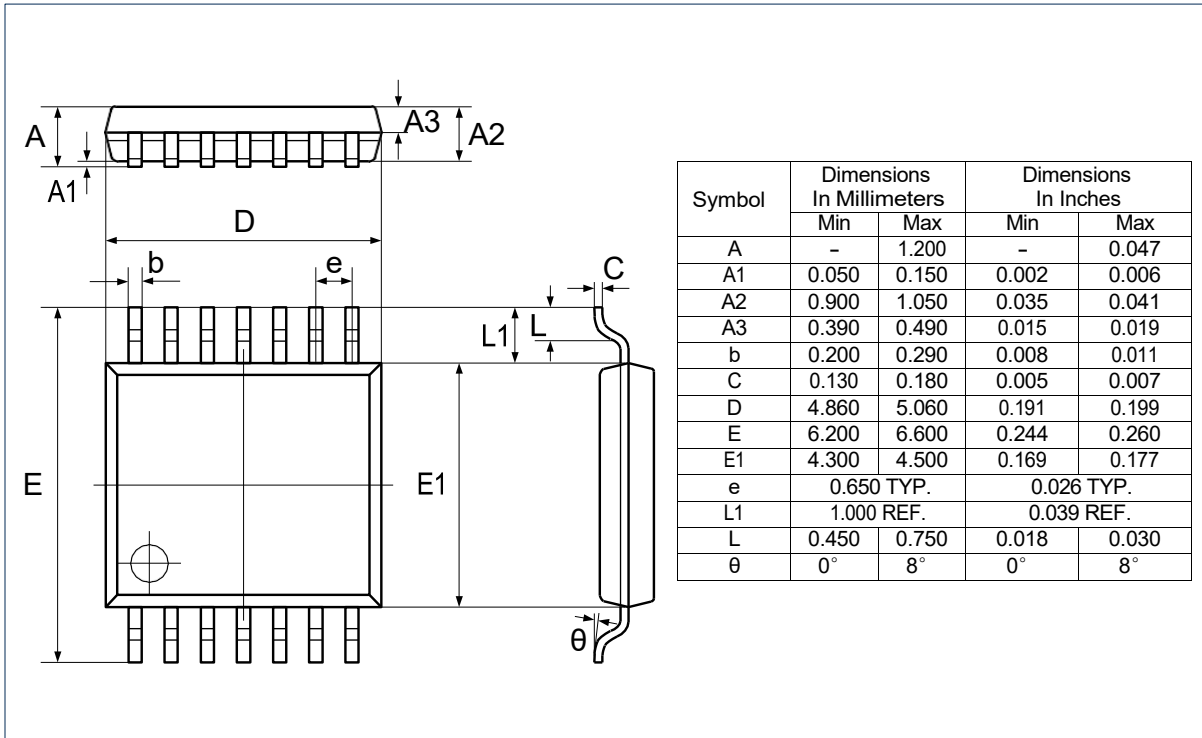
RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



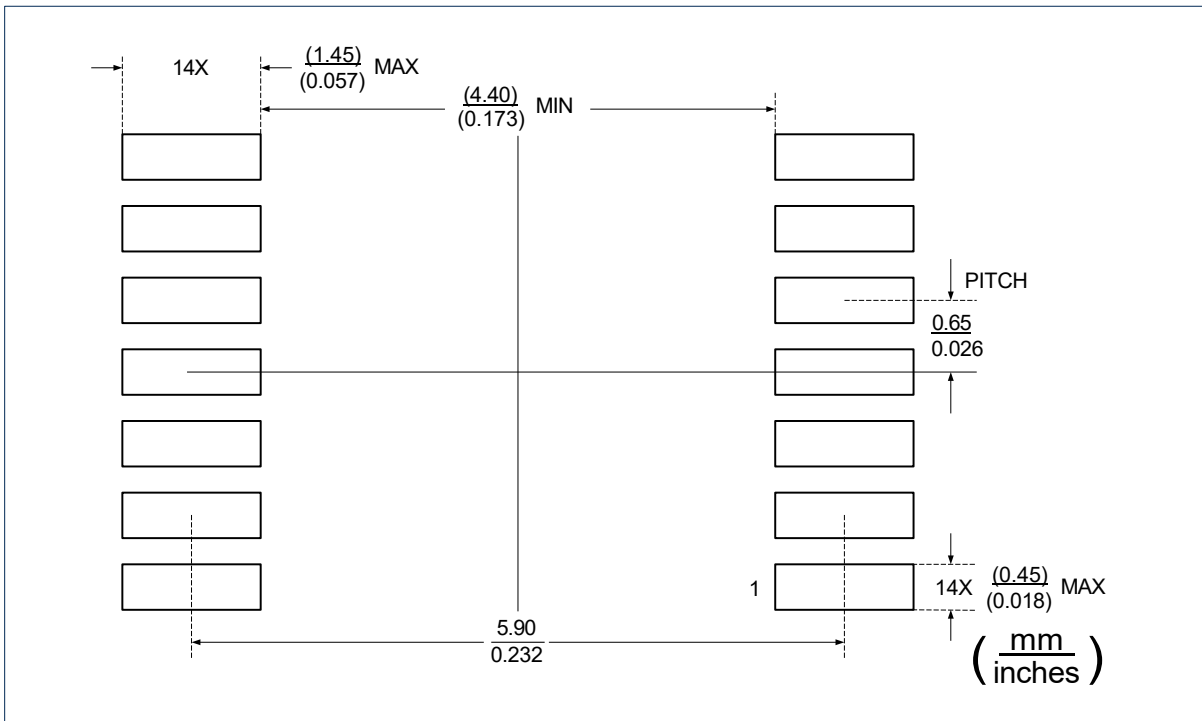
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Package Outlines (continued)

DIMENSIONS, ETSSOP-14L



RECOMMENDED SOLDERING FOOTPRINT, ETSSOP-14L



## Important Notice

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