

General Description

The LTP755L series are CMOS-based low-dropout, low-power linear regulators, offering 500mA with low dropout voltage, high ripple rejection, high output accuracy and low supply current. The LTP755L series consist of an accurate voltage-reference block, an error amplifier, a voltage -setting resistor net, a P-MOSFET pass device, a thermal-shutdown circuit and a current limit circuit with short protection.

The LTP755L uses a type of outstanding CMOS process to minimize the supply current. A low on-resistance P-MOS pass device is equipped for lower dropout voltage. LTP755L also possess the EN (enable) function to save more energy and extend the battery life. The LTP755L series are available in SOT23-5L, DFN1x1-4L and DFN2x2-6L packages.

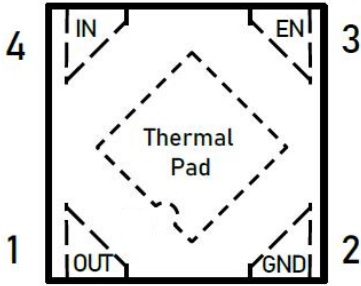
Features

- Input Voltage: 1.9V ~ 5.5V
- Output Current up to 500mA
- Low Supply Current: 50uA(typ)
- Excellent Load / Line Transient Response
- Build-in Auto-discharging circuit
- Build-in Over-current protection and Thermal-shutdown circuit
- Build-in Inrush-current suppression circuit and current limiter

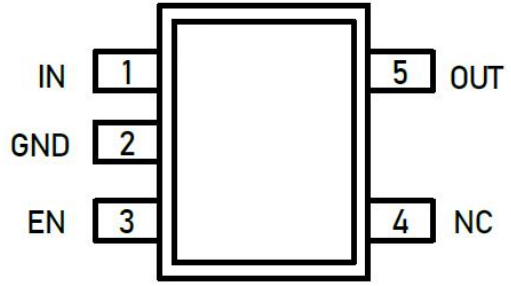
Pin Assignments

Type Number	Package Package Name	Package Name	Package Quantity
LTP755L	DFN1X1-4L	LTP755L-XXNXF4	Tape and Reel, 3000
	SOT23-5L	LTP755L-XXNXT5	Tape and Reel, 10000
	DFN2X2-6L	LTP755L-XXNXF6	Tape and Reel, 3000

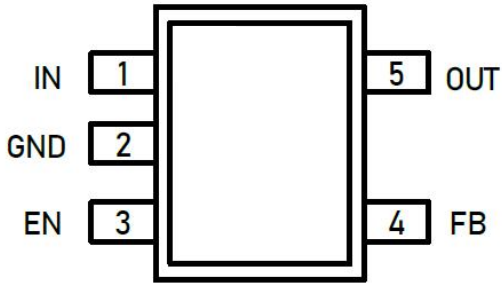
Pin Description (Top View)



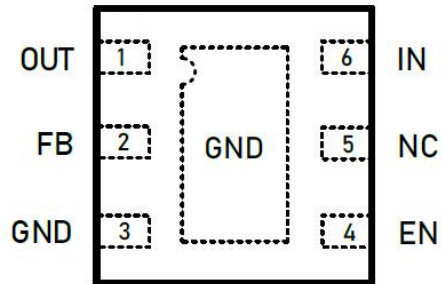
DFN1x1-4L(Fix Version)



SOT23-5L(Fix Version)



SOT23-5L(Adj Version)



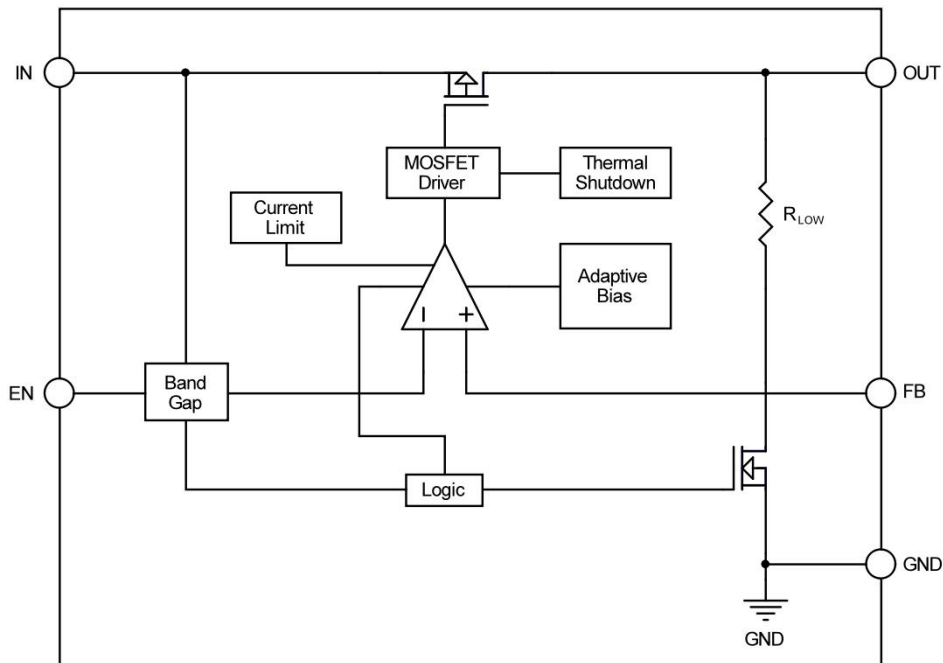
DFN2x2-6L(Adj Version)

Pin Function

Package				Symbol	Function
SOT23-5L(Fix)	SOT23-5L(Adj)	DFN1x1-4L	DFN2x2-6L		
2	2	2	3	GND	Ground.
1	1	4	6	IN	Supply input pin.
5	5	1	1	OUT	Output pin.
3	3	3	4	Note EN	Enable control input
4	/	/	5	NC	No Connection.
/	4	/	2	FB	Used to set the output voltage of the device
-	/	/	GND	GND	Ground
/	/	Thermal Pad	/	EPAD	Should be connected directly to the GND pin

Note: Enable Control Input, Active High, floating is not suggested.

Block Diagram



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Functional Description

Input Capacitor

A 2.2μF capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 2.2μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

EN Pin Operation

The LTP755L is turned on by setting the EN pin to “H”. Since the EN pin is neither pulled down or float, The LTP755L is closed.

Current Limit Protection

When output current of VOUT pin is higher than current limit threshold or the VOUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing to cool down. When the junction temperature reduce to approximately +130°C the output circuit is enabled again. Depending on power dissipation, thermal resistance and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of VOUT in very short time. The Auto-Discharging function is optional.

Output Voltage

The output voltage is adjustable using external 2 resistors. For better performance of the circuit, the R2 value need to be between 100kΩ and 1MΩ. The output voltage is calculated by:

$$V_{OUT} = (1+R1/R2) \times 0.8 \text{ (V)}$$

Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage (IN Pin)	-0.3 to 6.0	V
V_{EN}	Input Voltage (EN Pin) (If)	-0.3 to 6.0	V
V_{FB}	Input Voltage (FB Pin)	-0.3 to 6.0	V
V_{OUT}	Output Voltage (OUT Pin)	-0.3 to 6.0	V
T_J	Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
V_{ESD}	HBM (ANSI/ESDA/JEDEC JS-001)	3000	V
	CDM (ANSI/ESDA/JEDEC JS-002)	2000	V
I_{LU}	Latch up Current Maximum Rating (JESD78E)	± 200	mA

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	DFN1x1-4L	Thermal Characteristics, Thermal Resistance, Junction-to-Air	250	°C/W
	DFN2x2-6L		170	°C/W
	SOT23-5L		250	°C/W

Recommended Operating Conditions

Symbol	Parameters	Min	Max	Unit
V_{IN}	Input Voltage	1.9	5.5	V
I_{OUT}	Output Current	0	500	mA
T_A	Operating Ambient Temperature	-40	85	°C
C_{IN}	Input Ceramic Capacitor Value	0.47	10	uF
C_{OUT}	Output Ceramic Capacitor Value	0.47	10	uF
ESR	Input and Output Capacitor Equivalent Series Resistance	5	100	mΩ

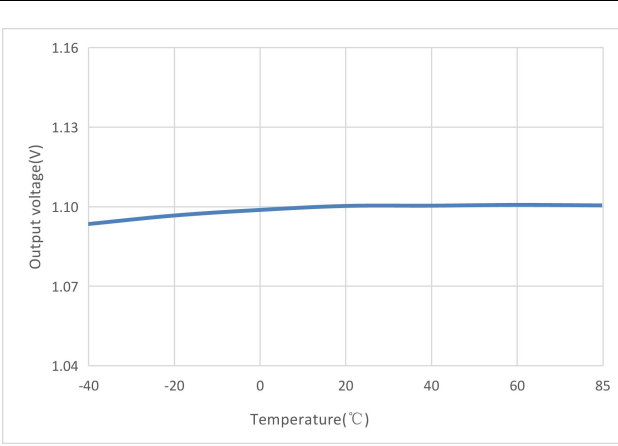
Electrical Characteristics

 $V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, (unless otherwise noted). $T_A = 25^\circ C$.

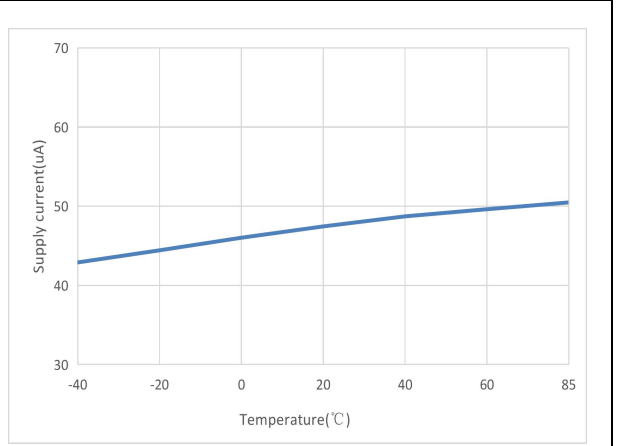
Symbol	Item	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		1.9		5.5	V
V_{OUT}	Output Voltage	$T_A = 25^\circ C$	-2		2	%
V_{FB}	FB Voltage (If FB Pin Exist)	$T_A = 25^\circ C$	0.784	0.800	0.818	V
		$T_A = -40^\circ C \sim 85^\circ C$	0.776	0.800	0.824	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$V_{IN} = V_{SET} + 1V$, $1mA \leq I_{OUT} \leq 0.5A$		20	50	mV
V_{DIF}	Dropout Voltage	$1.0V \leq V_{SET} < 1.6V$, $I_{OUT} = 0.5A$, V_{OUT} dropping to $0.98 \times V_{SET}$			900	mV
		$1.7V \leq V_{SET} < 2.6V$, $I_{OUT} = 0.5A$, V_{OUT} dropping to $0.98 \times V_{SET}$		350	500	mV
		$2.6 \leq V_{SET} < 3.6V$, $I_{OUT} = 0.5A$, V_{OUT} dropping to $0.98 \times V_{SET}$		260	400	mV
I_{SS}	Supply Current	$I_{OUT} = 0mA$		50	85	μA
$I_{Standby}$	Standby Current (If EN Pin Exist)	$V_{EN} = 0V$		0	1	μA
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$V_{SET} + 0.5V \leq V_{IN} \leq 5.5V$ ($V_{IN} \geq 1.4V$)		0.02		%/V
PSRR	Power Supply Rejection Ratio	$f = 1kHz$, Ripple $0.2Vp-p$, $V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 30mA$		70		dB
I_{LIM}	Output Current Limit	$V_{IN} = V_{SET} + 1V$		700	1200	mA
I_{Short}	Short Current Limit	$V_{OUT} = 0V$		150	240	mA
R_{PD}	EN Pull-down Resistance (If EN Pin Exist)			1M		Ω
V_{IH}	EN Input Voltage High (If EN Pin Exist)		0.9			V
V_{IL}	EN Input Voltage Low (If EN Pin Exist)				0.40	V
R_{DIS}	Auto-discharge Resistance (If EN Pin Exist)	$V_{IN} = 4V$, $V_{EN} = 0V$		80		Ω
T_{TSD}	Thermal Shutdown Temperature			155		$^\circ C$
T_{TSR}	Thermal Shutdown Released Temperature			130		$^\circ C$

Typical Characteristics

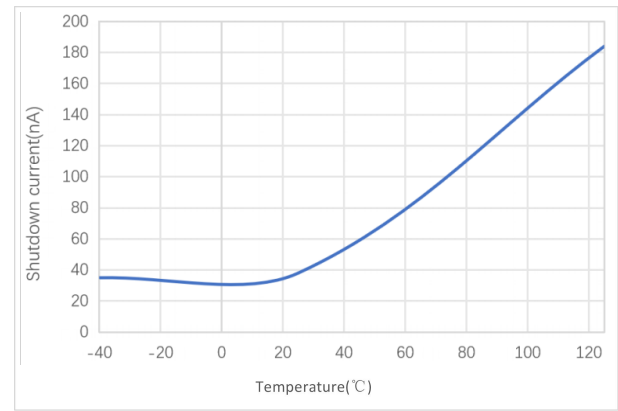
(1) VOLTAGE VERSION 1.1V, $V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, (unless otherwise noted). $T_A = 25^\circ C$.



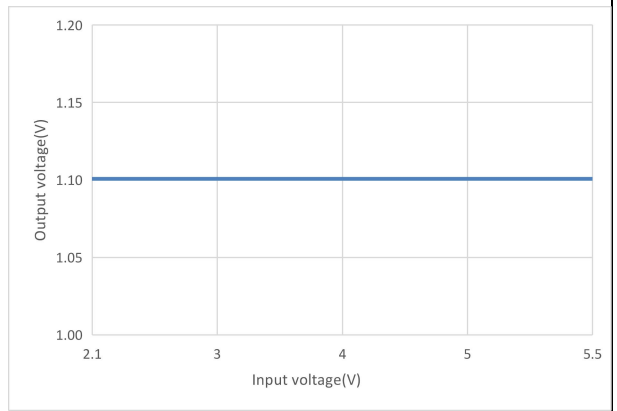
Output Voltage VS Temperature



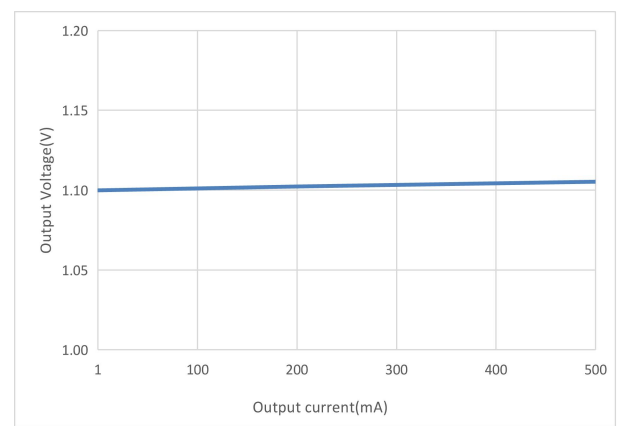
Supply Current VS Temperature



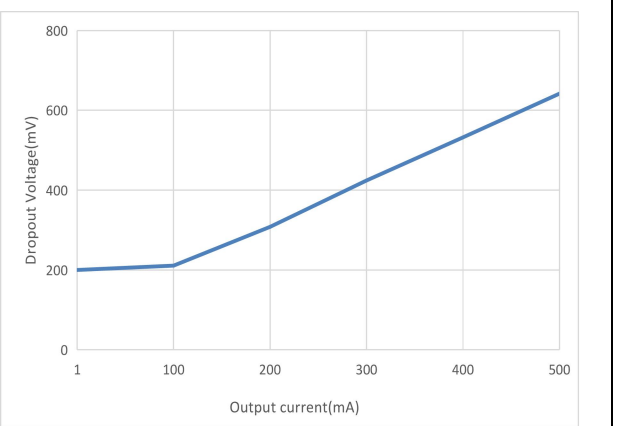
Shutdown Current VS Temperature



Output Voltage VS Input Voltage



Output Voltage VS Output Current

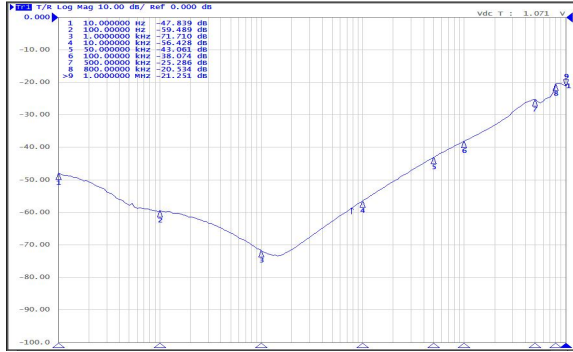


Dropout Voltage VS Output Current

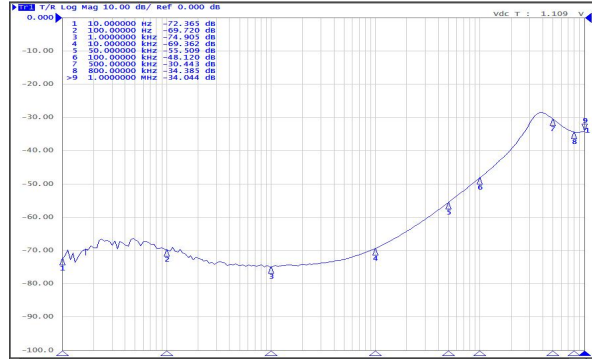
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Typical Characteristics (continued)

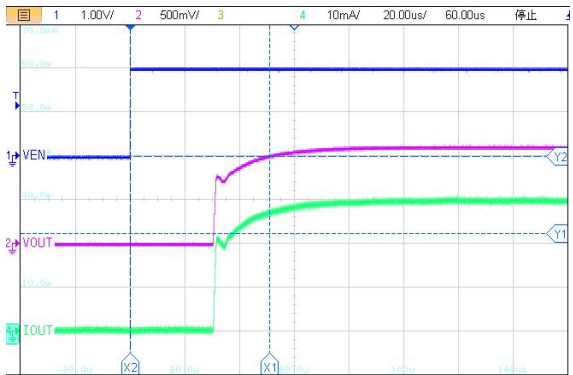
$V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, (unless other wise noted). $T_A = 25^\circ C$.



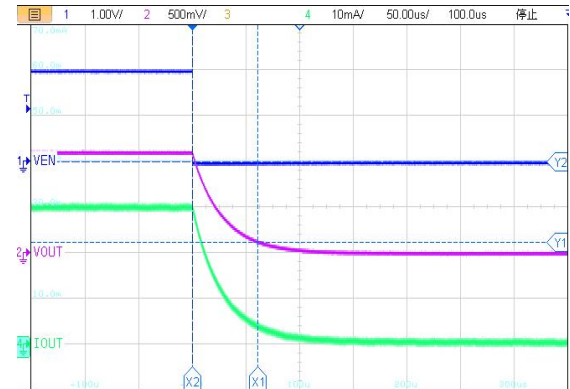
PSRR Test($I_{OUT}=30mA$)



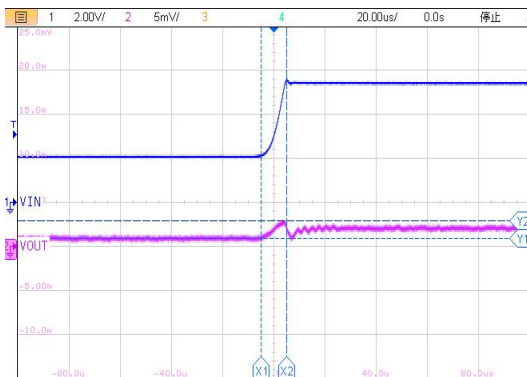
PSRR Test($I_{OUT}=0.5A$)



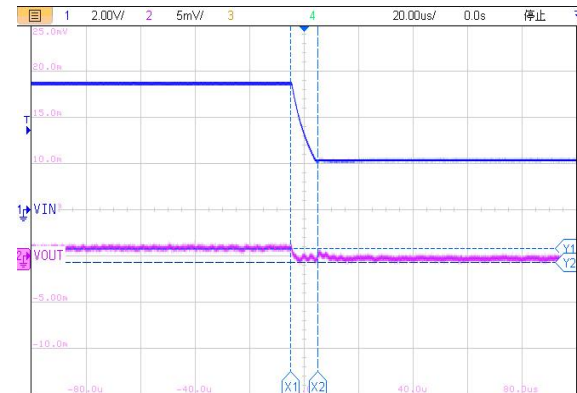
$t_{ON}=51\mu s(I_{OUT}=30mA)$



$t_{OFF}=61\mu s(I_{OUT}=30mA)$



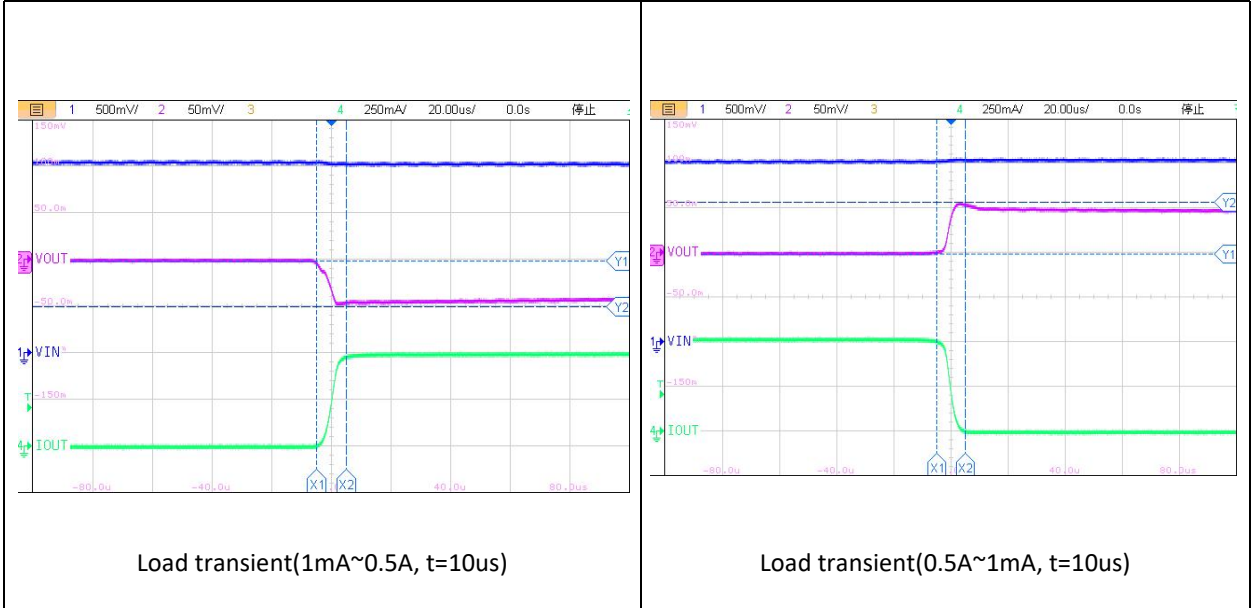
Line transient(2.1~5.5V, $t=10\mu s$)



Line transient(5.5~2.1V, $t=10\mu s$)

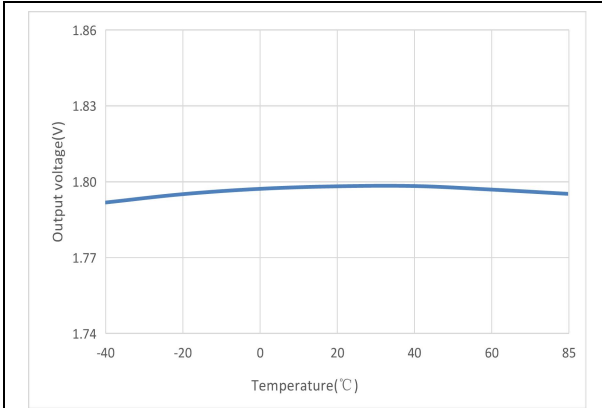
Typical Characteristics (continued)

$V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, (unless other wise noted). $T_A = 25^\circ C$.

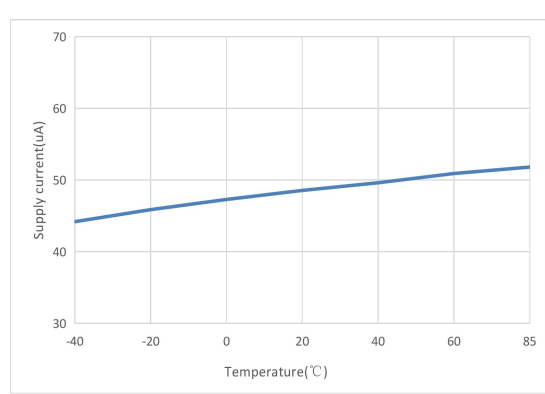


Typical Characteristics (continued)

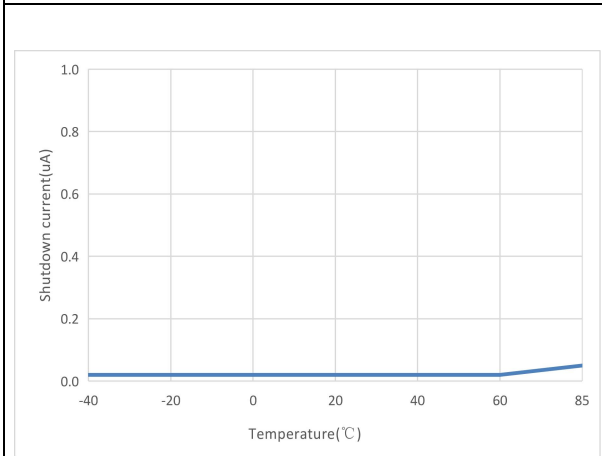
(2)VOLTAGE VERSION 1.8V, $V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, (unless otherwise noted). $T_A = 25^\circ C$.



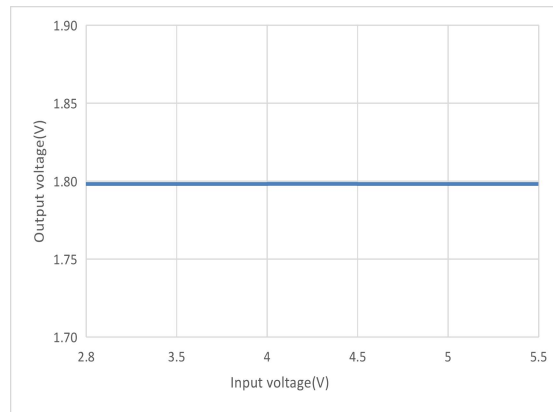
Output Voltage VS Temperature



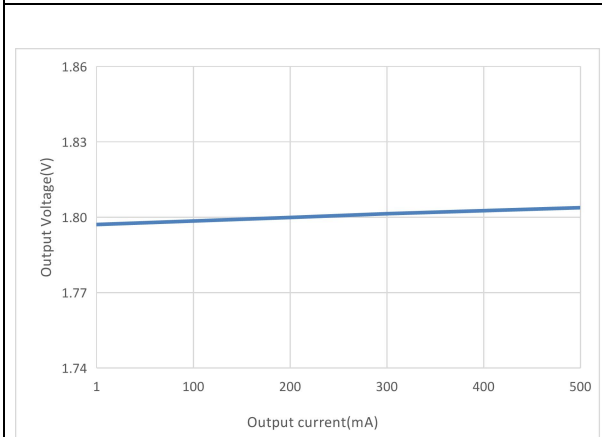
Supply Current VS Temperature



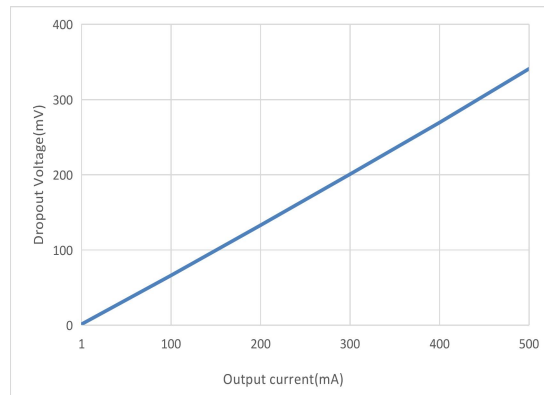
Shutdown Current VS Temperature



Output Voltage VS Input Voltage



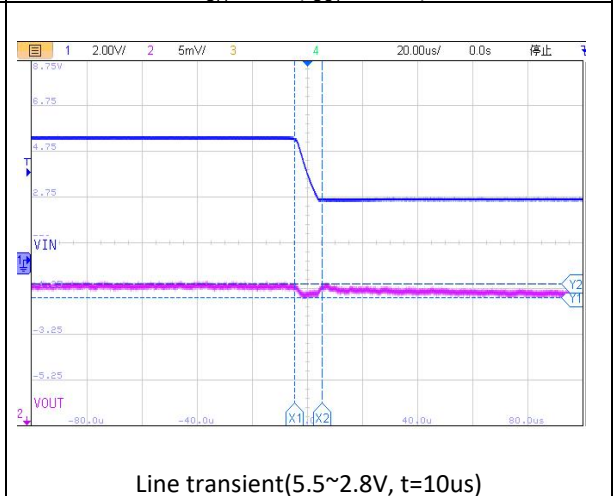
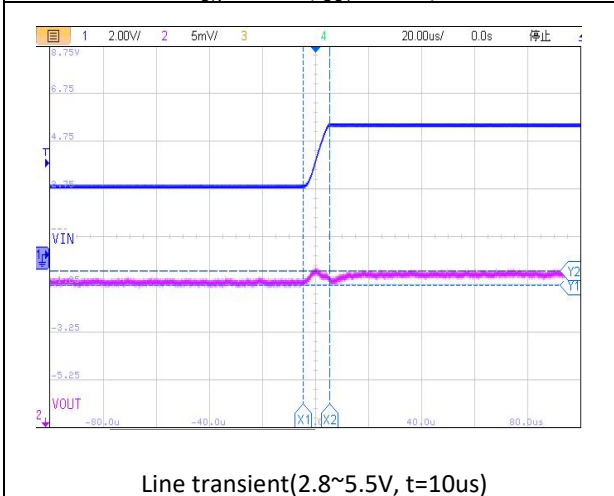
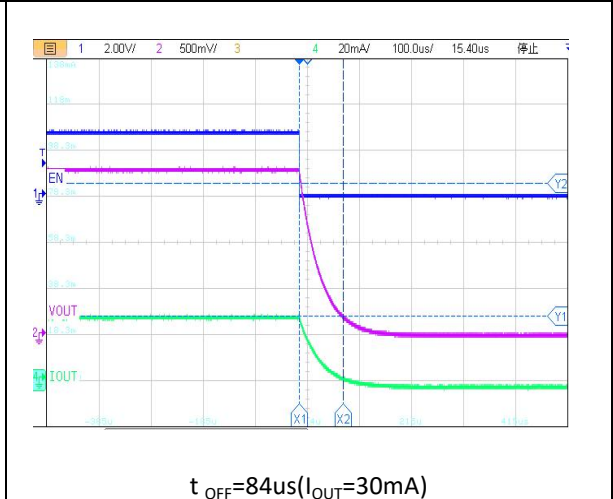
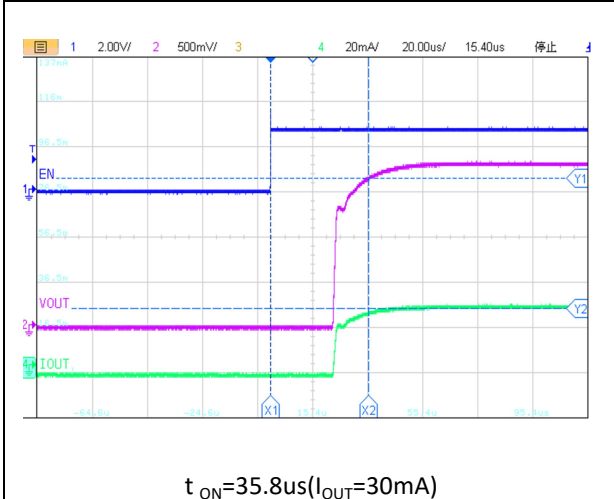
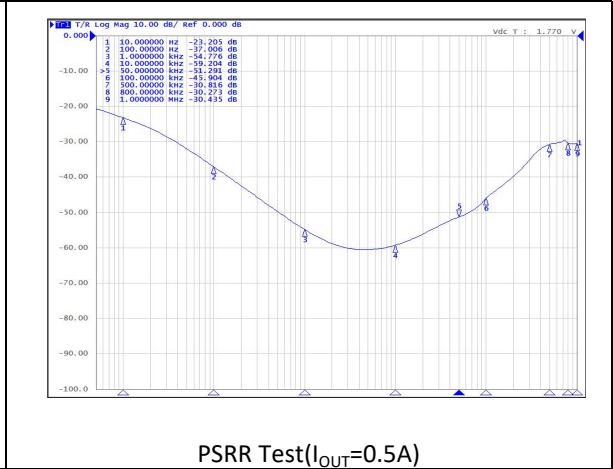
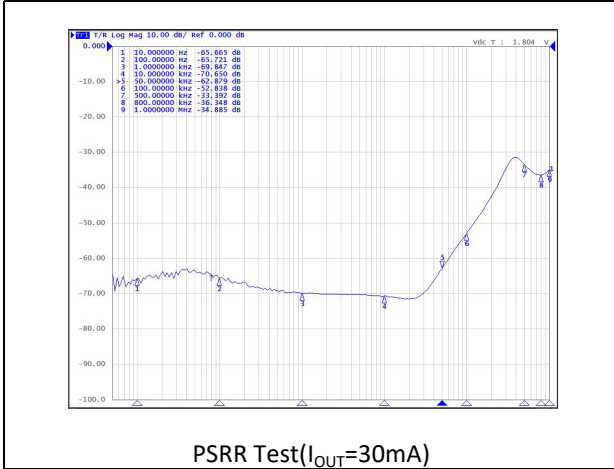
Output Voltage VS Output Current



Dropout Voltage VS Output Current

Typical Characteristics (continued)

$V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, (unless other wise noted). $T_A = 25^\circ C$.

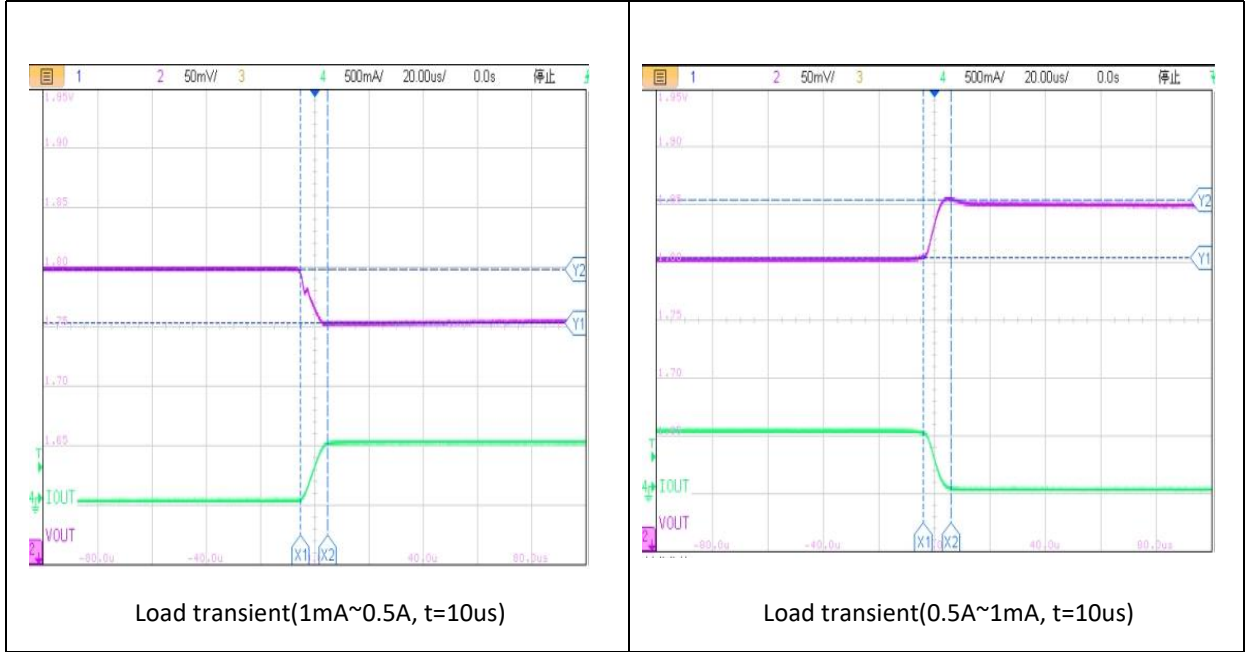


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Typical Characteristics (continued)

$V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, (unless otherwise noted). $T_A = 25^\circ C$.

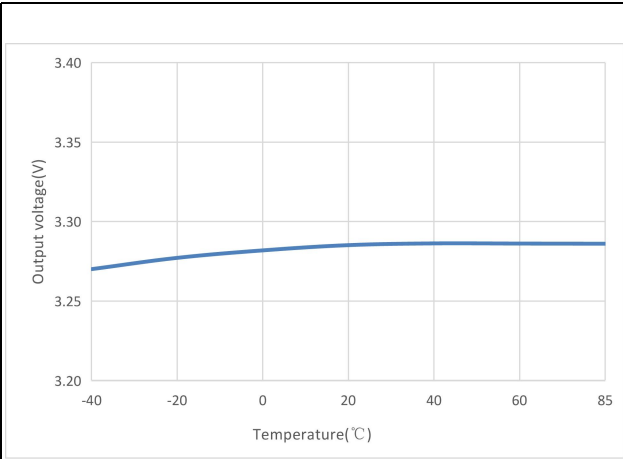


Load transient(1mA~0.5A, t=10us)

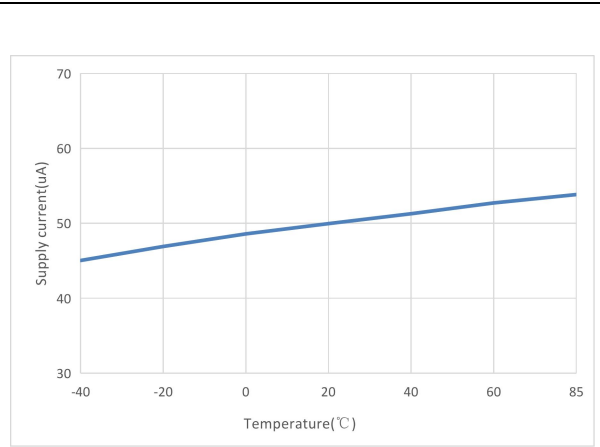
Load transient(0.5A~1mA, t=10us)

Typical Characteristics (continued)

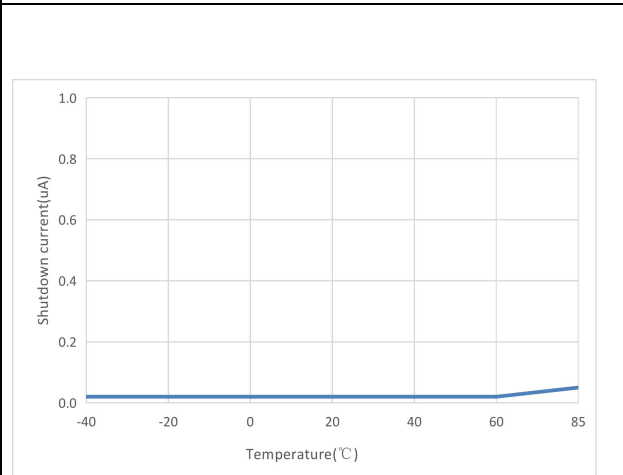
(3)VOLTAGE VERSION 3.3V, $V_{IN} = V_{SET} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, (unless otherwise noted). $T_A = 25^\circ C$.



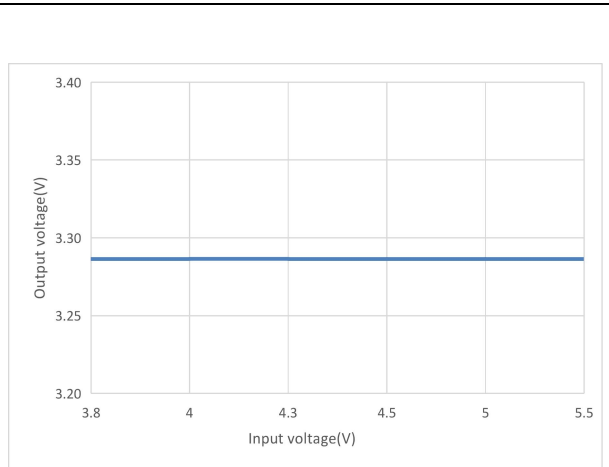
Output Voltage VS Temperature



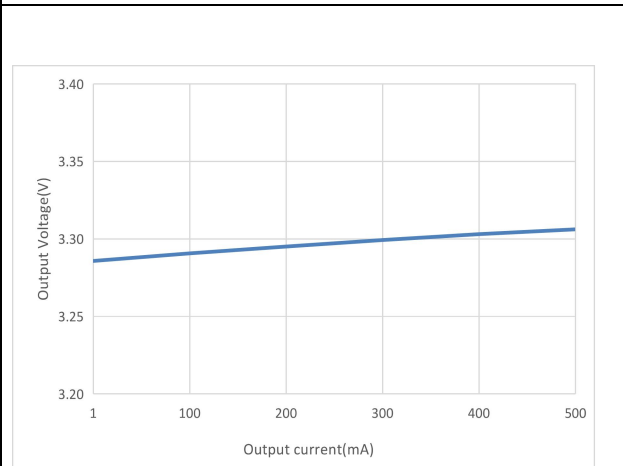
Supply Current VS Temperature



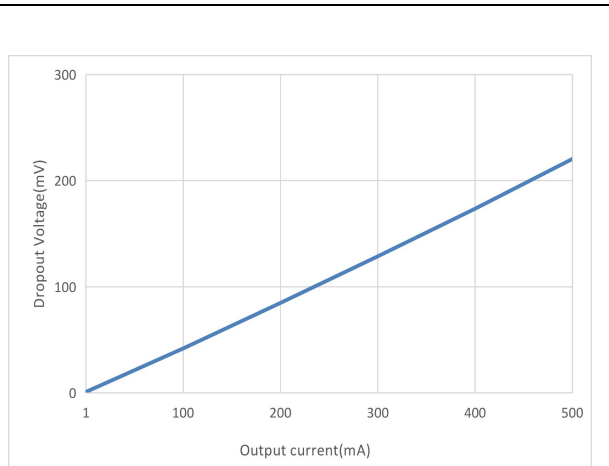
Shutdown Current VS Temperature



Output Voltage VS Input Voltage



Output Voltage VS Output Current

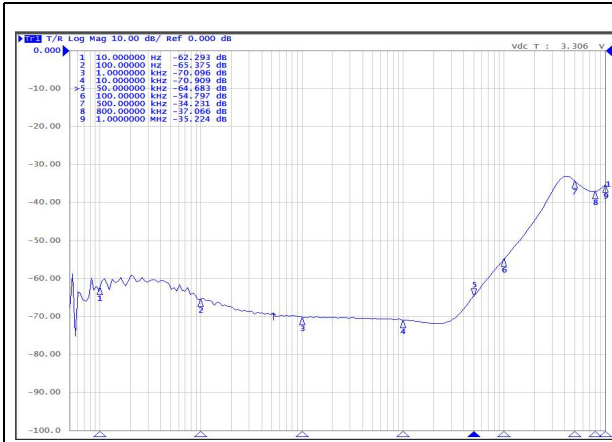


Dropout Voltage VS Output Current

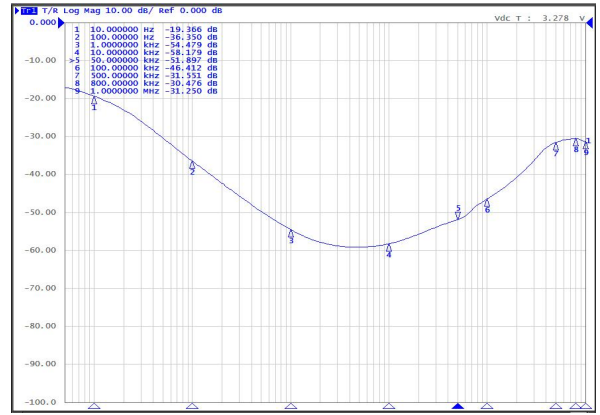
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Typical Characteristics (continued)

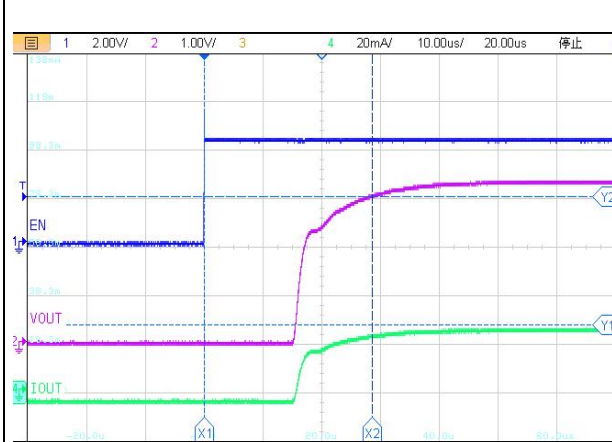
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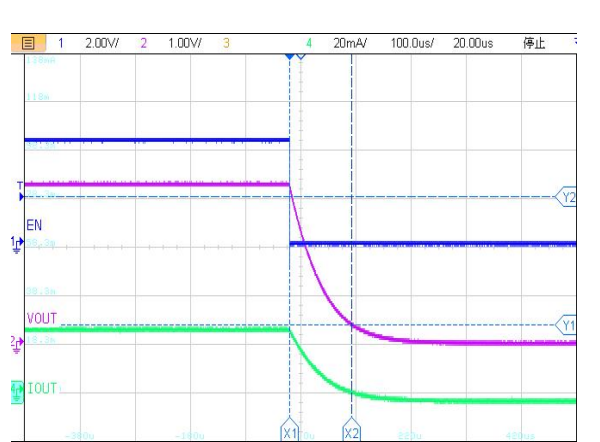
PSRR Test($I_{OUT}=30mA$)



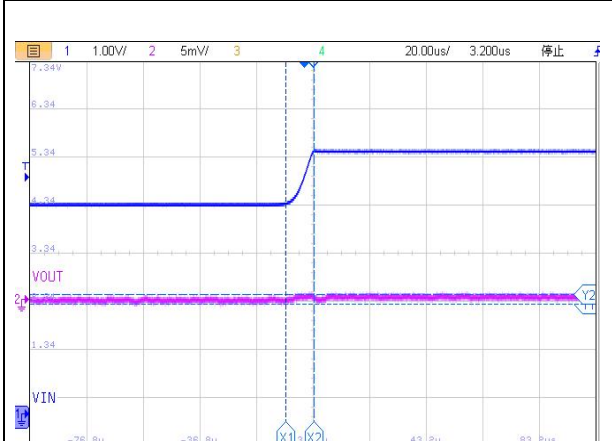
PSRR Test($I_{OUT}=0.5A$)



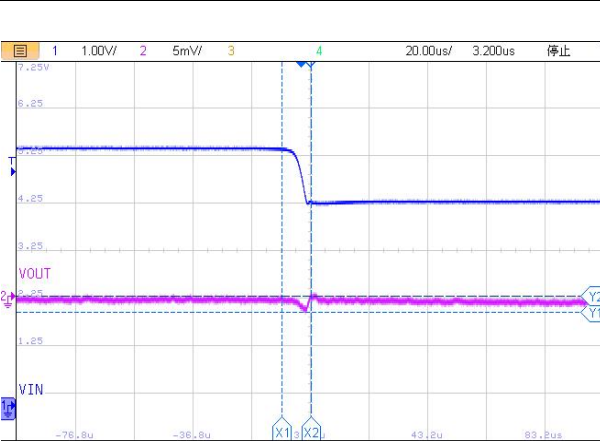
$t_{ON}=28.6\mu s(I_{OUT}=30mA)$



$t_{OFF}=112\mu s(I_{OUT}=30mA)$



Line transient(4.3~5.5V, $t=10\mu s$)



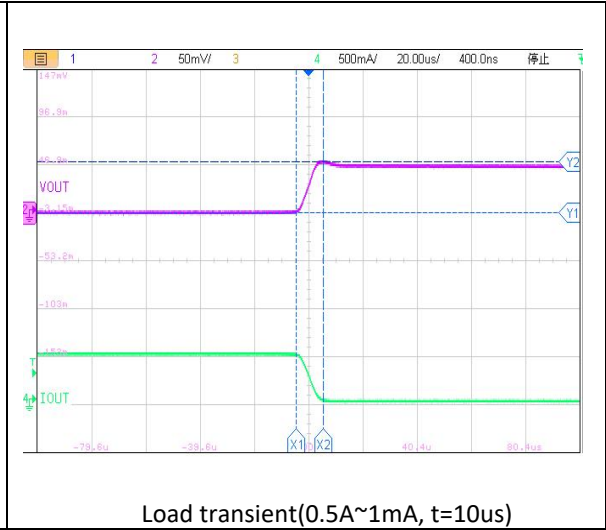
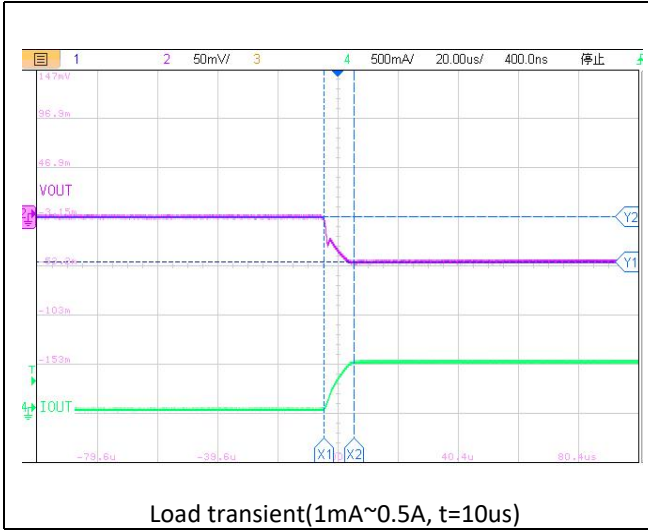
Line transient(5.5~4.3V, $t=10\mu s$)

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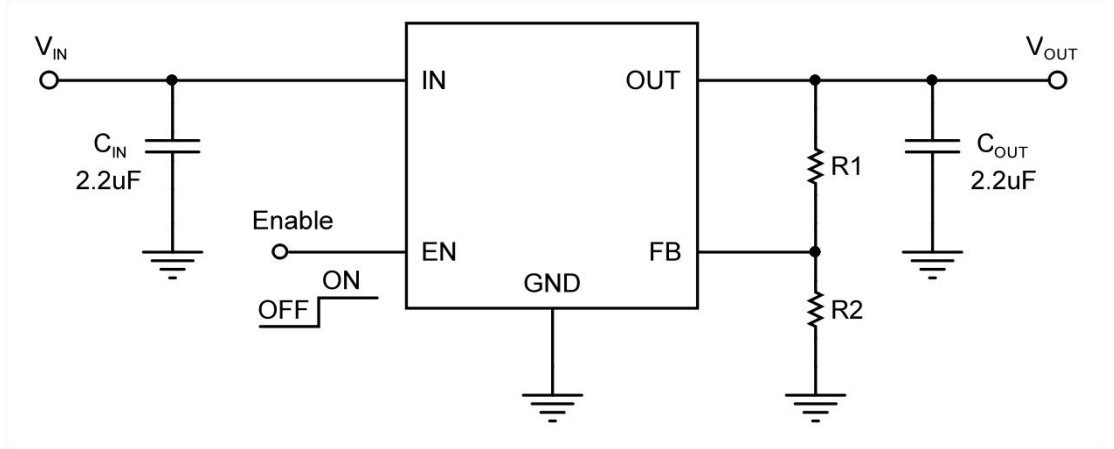


Typical Characteristics (continued)

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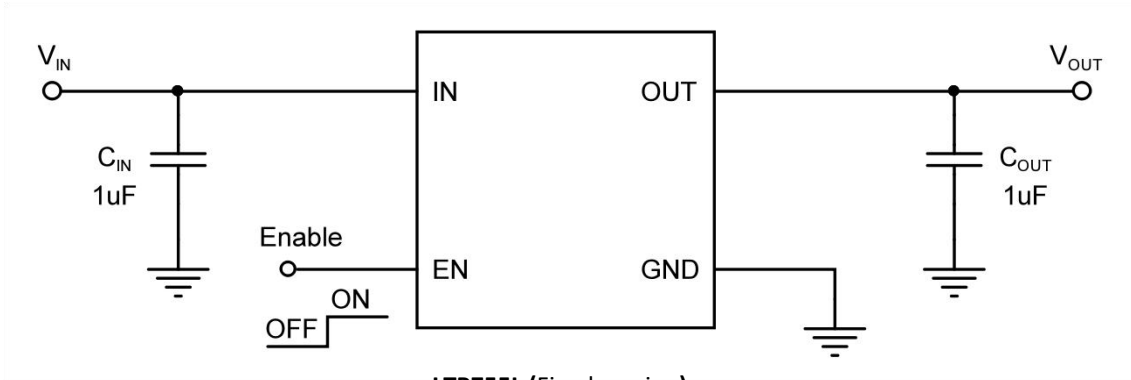


Application Circuits

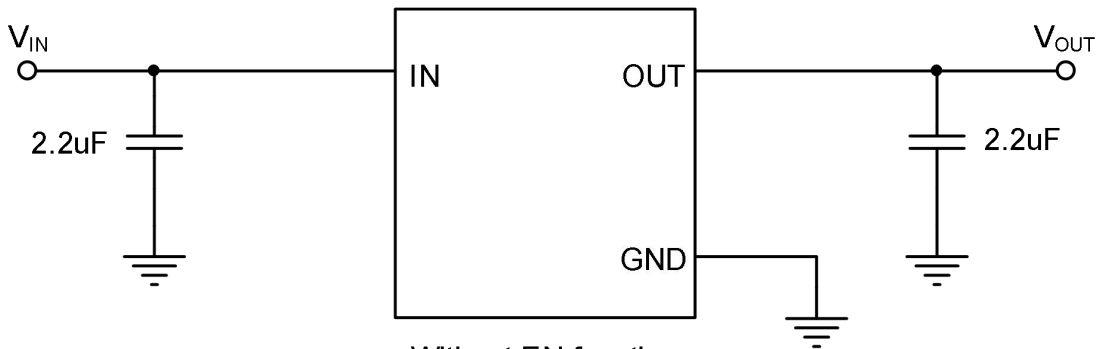


LTP755L-ADJ (ADJ version)

*: $V_{OUT} = (1 + R1/R2) \times 0.8V$, R2 recommend 100KΩ ~ 1MΩ.



LTP755L (Fixed version)

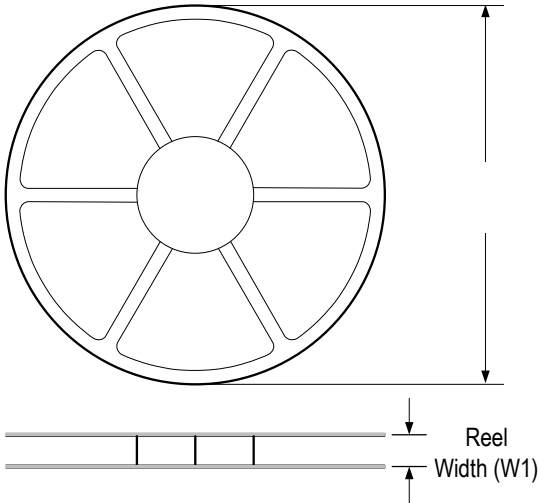


Without EN function

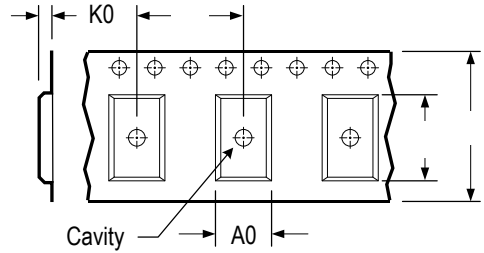
LTP755L (Fixed version)

Tape and Reel Information

REEL DIMENSIONS

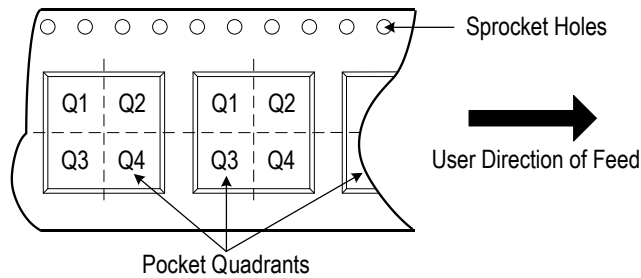


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



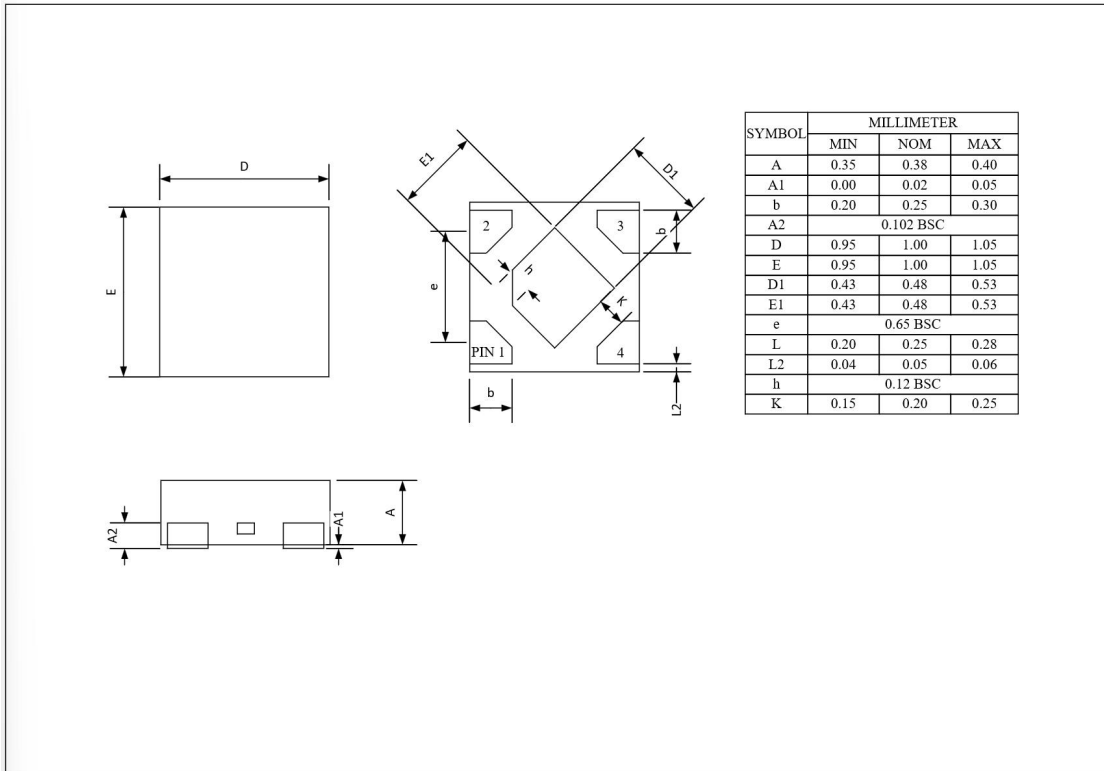
* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTP755L-xxNXF6	DFN2×2	6	3 000	178	9.5	2.25	2.25	1.0	4.0	8.0	Q1
LTP755L-xxNXT5	SOT23	5	10 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTP755L-xxNXF4	DFN1×1	4	3 000	178	9.5	1.1	1.1	0.5	2.0	8.0	Q1

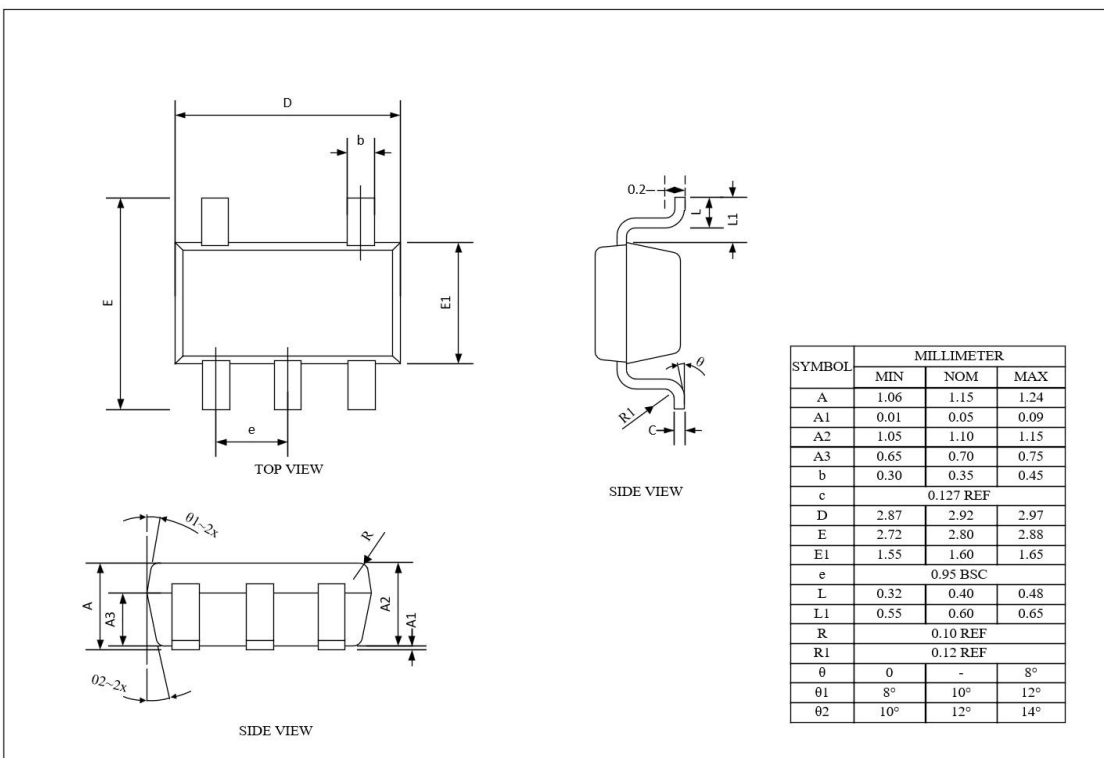
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Package Dimension

DFN1x1-4L



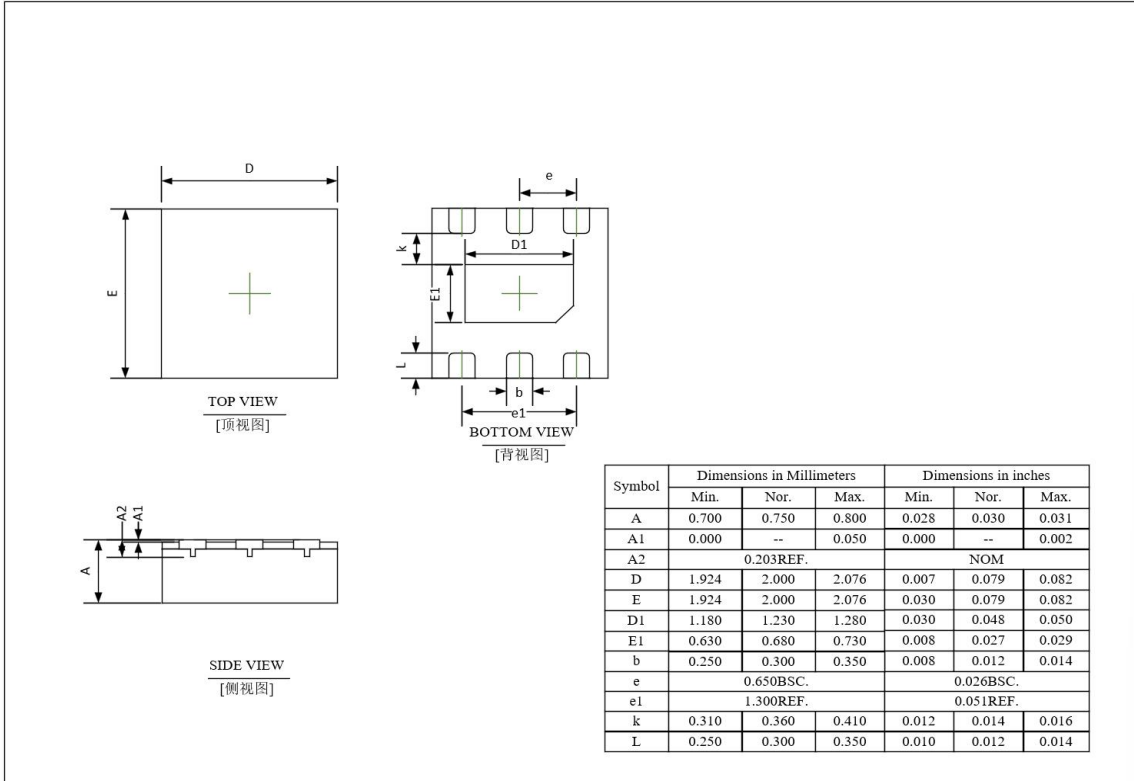
SOT23-5L



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Package Dimension

DFN2x2-6L



Important Notice

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