General Description

The LTA1240 device is a voltage-output, current-sensing amplifier with enhanced PWM rejection, capable of detecting the voltage drop across a shunt resistor within a wide common-mode voltage range of –4V to 100V independent of the supply voltage. The negative common-mode voltage allows the device to operate below ground, accommodating flyback cycles in typical solenoid applications. This feature enables precise current measurement without causing significant output voltage transients and associated recovery ripple.

The device operates from a single supply voltage of 2.7V to 5.5V, consuming a maximum supply current of 2.4mA. The low offset of the zero-drift architecture allows current sensing even with a shunt voltage drop as low as 10mV. All versions offer an extended operating temperature range of -40°C to +125°C and are available in SOIC-8L packages.

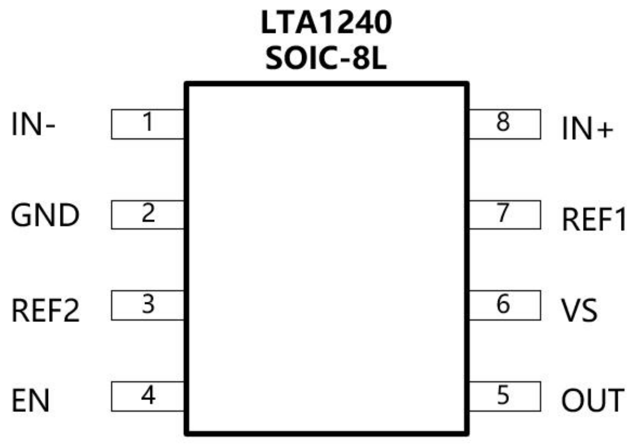
Features and Benefits

- Enhanced PWM Suppression
- Excellent Common-Mode Rejection Ratio (CMRR):
  - 132dB DC CMRR
  - 68dB AC CMRR (at 50kHz)
- Wide Common-Mode Range: -4V to 100V
- Accuracy:
  - Gain: 20V/V
    Gain Error: ±0.20% (max)
    Gain Drift: ±2.5ppm/°C (max)
  - Offset:
    Offset Voltage: ±25μV (max)
    Temperature Drift: ±500nV/°C (max)
- Quiescent Current: 2.4mA (max)

Applications

- Motor Control
- Solenoid and Valve Control
- Power Management
- Actuator Control
- Pressure Regulator
- Telecommunication Equipment

Pin Description (Top View)



Pin Function

PackageNC	Symbol	Function
1	IN-	Inverting input of the amplifier.
2	GND	Ground.
3	REF2	Reference voltage 2.
4	EN	Device enable. Pull EN above the specified threshold or leave EN floating to enable the Device.
5	OUT	Amplifier output.
6	VS	Power supply.
7	REF1	Reference voltage 1.
8	IN+	Non-inverting input of the amplifier.

Ordering Information

Package Type	Part Number	Quantity	Mark Code
SOIC-8L	LTA1240A2XS8/R8	Tape and Reel, 4 000	NA1A2

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Power supply voltage			6	V
Simulated input, V_{IN+}, V_{IN-}	Differential (V_{IN+}) - (V_{IN-})	-40	40	V
	Common mode	-4	100	V
REF1, REF2, EN input		GND-0.3	V_S+0.3	V
Output		GND-0.3	V_S+0.3	V
Operating Temperature Range, T_A		-55	150	℃
Operating Junction Temperature Range, T_J			150	℃
Storage Temperature Range, T_{stg}		-65	150	℃

ESD Ratings

Parameter	Level	Unit
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2 000	V
Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	±2 000	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CM}	Common-mode input voltage	-4	100	V
V_S	Operating power voltage	2.7	5.5	V
T_A	Operating Temperature Range	-40	+125	℃

Electrical Characteristics

At T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} – V_{IN-}, V_{CM} = 12V and V_{REF1} = V_{REF2} = V_S/2 (unless otherwise specified).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT						
Common-mode voltage range	V_{CM}	V_{IN+} = –4V to 100V, V_{SENSE} = 0mV, T_A = –40°C to +125°C	-4		100	V
Common-mode rejection ratio	CMRR	V_{IN+} = –4V to 100V, V_{SENSE} = 0mV, T_A = –40°C to +125°C	120	132		dB
		f = 50kHz		68		
Input offset voltage	V_{OS}	V_{SENSE} = 0mV		±5	±25	µV
Input Offset Voltage vs Temperature	dV_{OS} / dT	V_{SENSE} = 0mV, T_A = -40 to +125 °C		±50	±500	nV/°C
Power supply rejection ratio	PSRR	V_S = 2.7V to 5.5V, V_{SENSE} = 0mV, T_A = –40°C to 125°C		±1	±10	µV/V
Input bias current	I_B	I_{B+}, I_{B-}, V_{SENSE} = 0mV		90		µA
Reference input range			0		V_S	V
OUTPUT						
Gain	G	LTA1240A2		20		V/V
Gain Error		GND + 50mV ≤ V_{OUT} ≤ V_S – 200mV		±0.1	±0.20	%
		T_A = – 40°C - 125°C		±0.5	±2.5	ppm/°C
Nonlinearity Error		GND + 50mV ≤ V_{OUT} ≤ V_S – 200mV		±0.01		%
Reference divider accuracy		V_{OUT} = | (V_{REF1} – V_{REF2}) | / 2 at V_{SENSE} = 0 mV, T_A = –40°C to 125°C		0.02	0.1	%
Reference voltage rejection ratio (input-referred)	RVRR	LTA1240A2		40		µV/V
Maximum capacitive load		No sustained oscillation		0.47		nF
VOLTAGE OUTPUT						
Swing to V_S power-supply rail	V_{OH}	R_L = 10 kΩ to GND, T_A = –40°C to 125°C		V_S – 0.05	V_S – 0.2	V
Swing to GND	V_{OL}	R_L = 10 kΩ to GND, V_{SENSE} = 0 mV, V_{REF1} = V_{REF2} = 0 V, T_A = –40°C to 125°C		V_{GND} + 1	V_{GND} + 10	mV
FREQUENCY RESPONSE						
Band Width	BW	-3-dB Bandwidth		400		kHz
Slew Rate	SR			7		V/µs
Settling time				1		µs
NOISE (INPUT REFERRED)						
Voltage noise density	e_n			55		nV/√Hz

Electrical Characteristics (Cont.)

At T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} – V_{IN-}, V_{CM} = 12V and V_{REF1} = V_{REF2} = V_S/2 (unless otherwise specified).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Operating supply voltage	V_S	T_A = –40°C to +125°C	2.7		5.5	V
Quiescent current (per amplifier)	I_Q	V_{SENSE} = 0mV		1.8	2.4	mA
		T_A = –40°C to +125°C			2.6	mA
Shutdown current	I_{SD}	V_{EN} = 0V		1.2		mA
ENABLE						
EN up threshold	V_{ENH}		2.6			V
EN down threshold	V_{ENL}				1.2	V
EN pull-up current	I_{ENS}			2		μA
THERMAL CHARACTERISTICS						
Operating temperature range	T_A		-40		+125	°C
Package Thermal Resistance	θ_{JA}	SOIC-8L		125		°C /W

Typical Performance Characteristics

At T_A = 25°C, V_S = 5V, $V_{SENSE} = V_{IN+} - V_{IN-}$, V_{CM} = 12V and $V_{REF1} = V_{REF2} = V_S/2$ (unless otherwise specified).

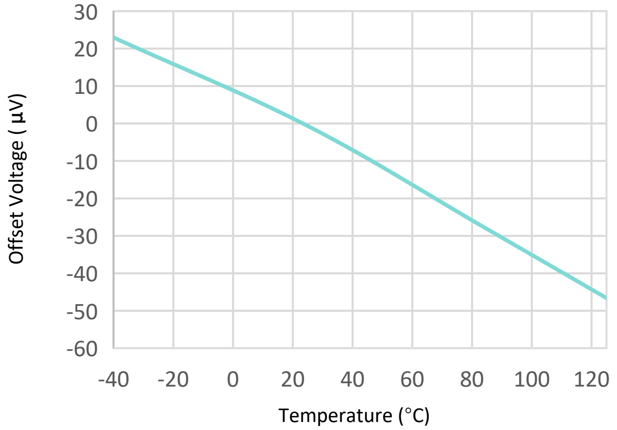


Figure 1. Offset Voltage vs Temperature.

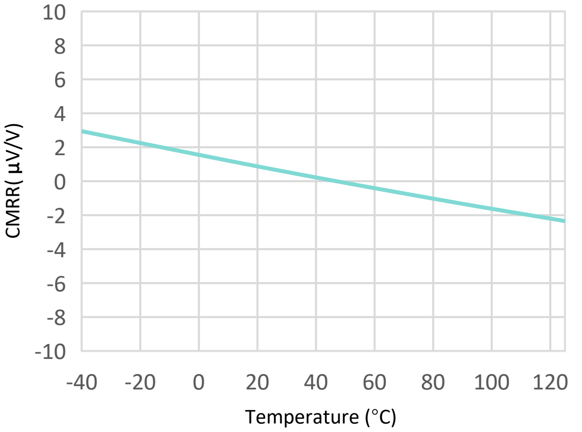


Figure 2. Common-Mode Rejection Ratio vs Temperature.

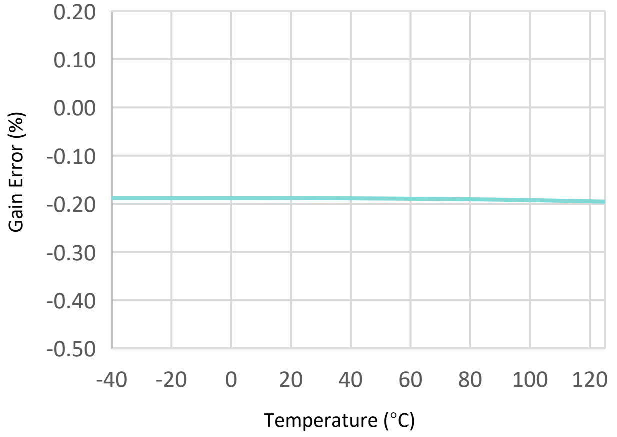


Figure 3. Gain Error vs Temperature.

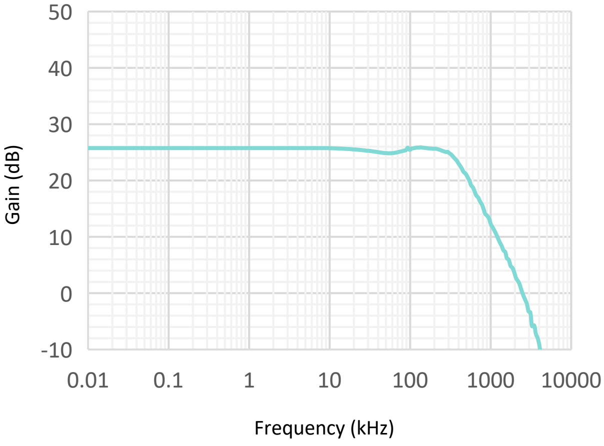


Figure 4. Gain vs Frequency.

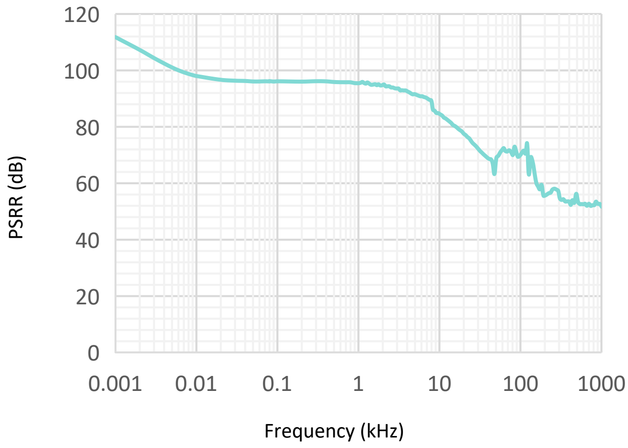


Figure 5. Power-Supply Rejection Ratio vs Frequency.

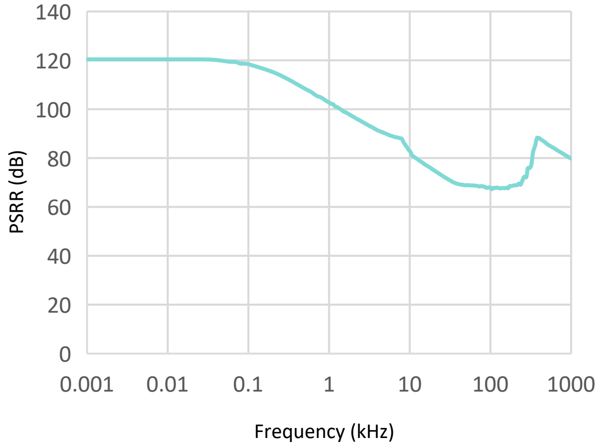


Figure 6. Common-Mode Rejection Ratio vs Frequency.

Typical Performance Characteristics (Cont.)

At T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} − V_{IN-}, V_{CM} = 12V and V_{REF1} = V_{REF2} = V_S/2 (unless otherwise specified).

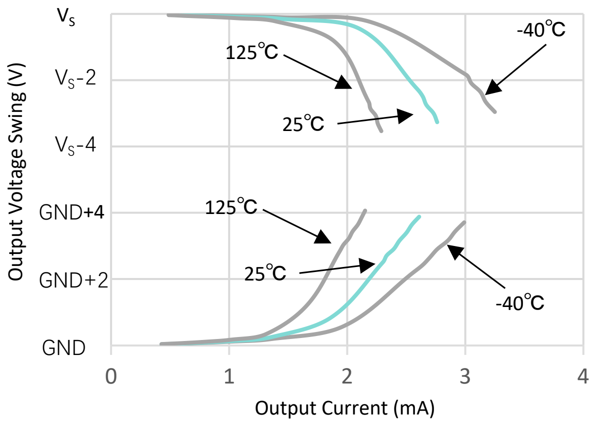


Figure 7. Output Voltage Swing as a function of Output Current.

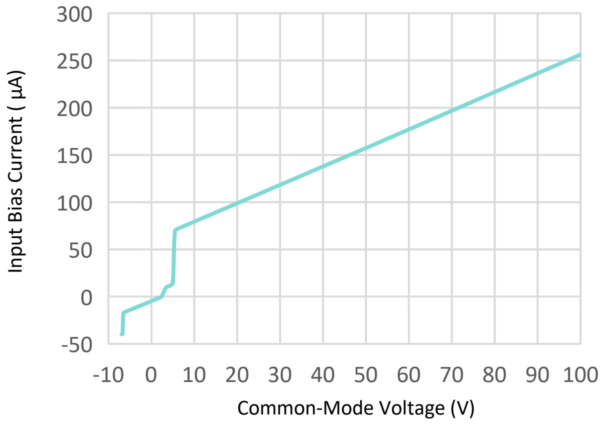


Figure 8. Input Bias Current vs Common-Mode Voltage (V_S=5V).

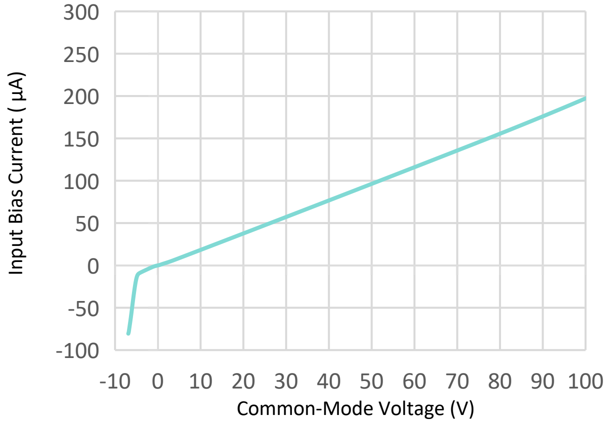


Figure 9. Input Bias Current vs Common-Mode Voltage (V_S=0V).

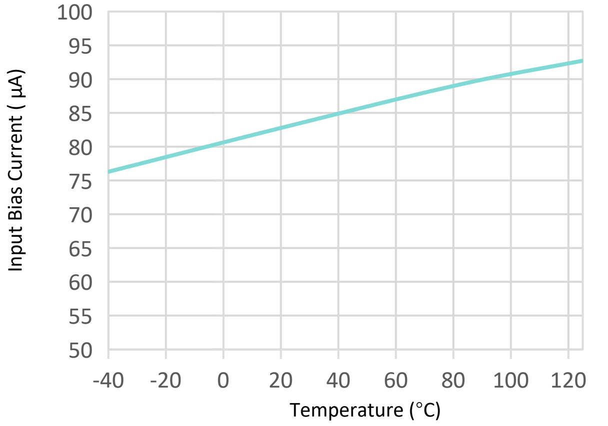


Figure 10. Input Bias Current vs Temperature.

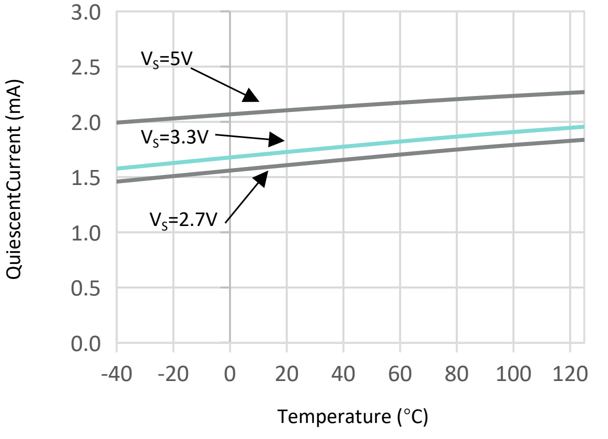


Figure 11. Quiescent Current vs Temperature.

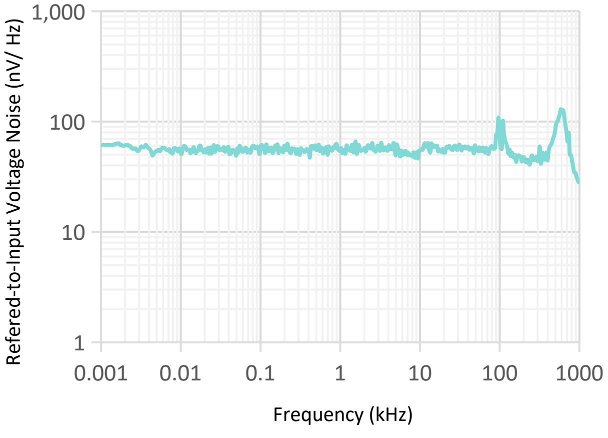


Figure 12. Input-Referred Voltage Noise vs Frequency.

Typical Performance Characteristics (Cont.)

At T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} − V_{IN-}, V_{CM} = 12V and V_{REF1} = V_{REF2} = V_S/2 (unless otherwise specified).

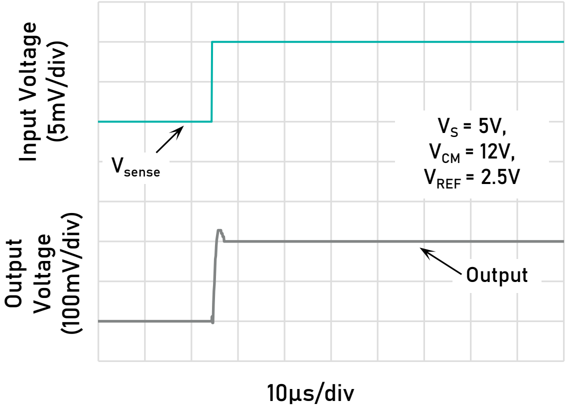


Figure 13. Step Response.

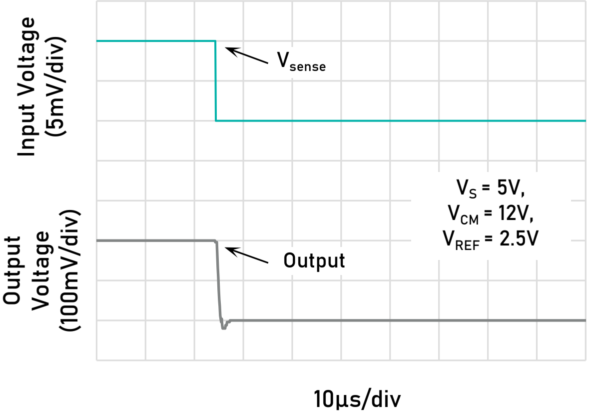


Figure 14. Step Response.

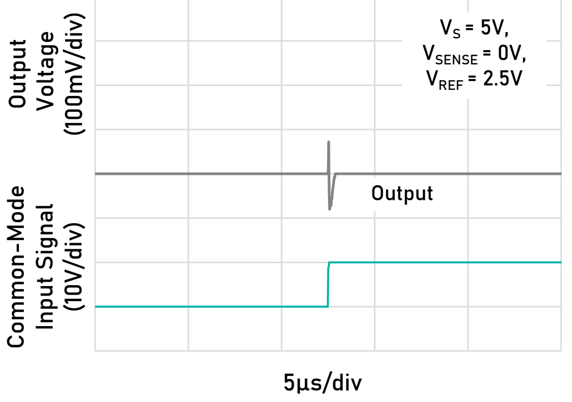


Figure 15. Common-Mode Voltage Transient Response.

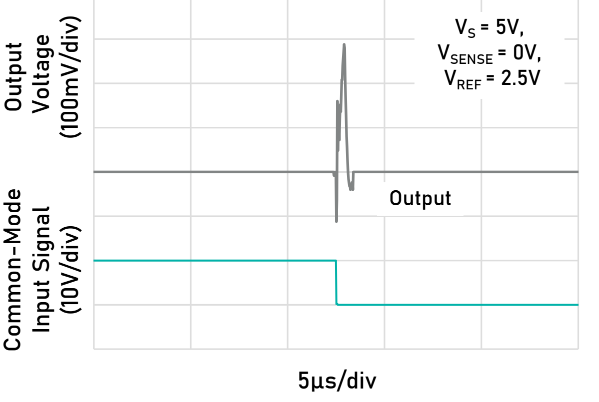


Figure 16. Common-Mode Voltage Transient Response.

Detailed Description

Overview

The LTA1240 is a current-sense amplifier that offers a wide common-mode range, precision, zero-drift topology, excellent common-mode rejection ratio (CMRR) and features enhanced pulse width modulation (PWM) rejection. Enhanced PWM rejection reduces the effect of common-mode transients on the output signal that are associated with PWM signals. Multiple gain versions are available to allow for the optimization of the desired full-scale output voltage based on the target current range expected in the application.

Functional Block Diagram

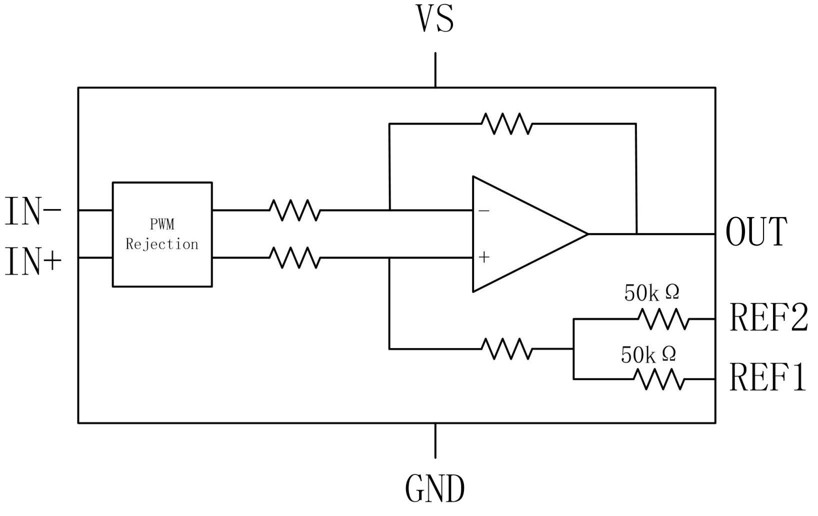


Figure 17: Functional Block Diagram

Application and Implementation

Application Information

The LTA1240 measures the voltage developed as current flows across the current-sensing resistor. The device provides reference pins to configure operation as either unidirectional or bidirectional output swing. When using the LTA1240 for inline motor current sense, the device is commonly configured for bidirectional operation.

Input Filtering

Based strictly on user design requirements, external filtering of the current signal may be desired. The initial location that can be considered for the filter is at the output of the current amplifier. Although placing the filter at the output satisfies the filtering requirements, this location changes the low output impedance measured by any circuitry connected to the output voltage pin. The other location for filter placement is at the current amplifier input pins. This location satisfies the filtering requirement also, however the components must be carefully selected to minimally impact device performance. Figure 18 shows a filter placed at the inputs pins.

Application and Implementation (Cont.)

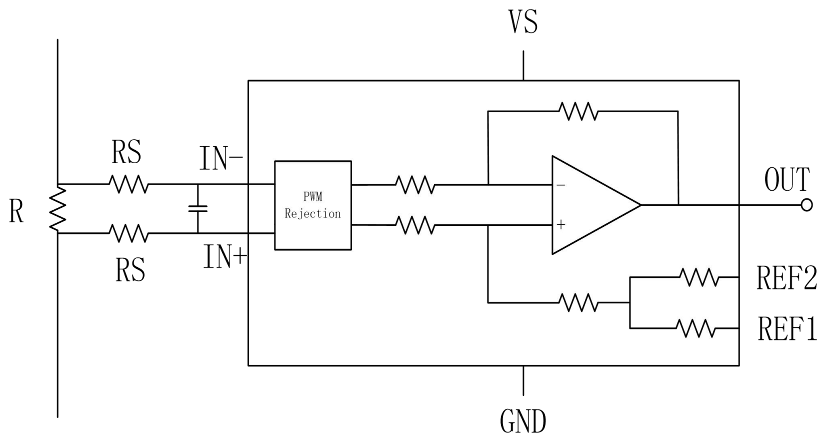


Figure 18： Filter at Input Pins

External series resistance provide a source of additional measurement error, so keep the value of these series resistors to 10Ω or less to reduce loss of accuracy. The internal bias network shown in Figure 18 creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, a mismatch is created in the voltage drop across the filter resistors. This voltage is a differential error voltage in the shunt resistor voltage. In addition to the absolute resistor value, mismatch resulting from resistor tolerance can significantly impact the error because this value is calculated based on the actual measured resistance.

The measurement error expected from the additional external filter resistors can be calculated using Equation 1, where the gain error factor is calculated using Equation 2.

$$\text{Equation 1:} Gain\ Error\ (\%) = 100 - (100 * Gain\ Error\ Factor)$$

The gain error factor, shown in Equation 1, can be calculated to determine the gain error introduced by the additional external series resistance. Equation 1 calculates the deviation of the shunt voltage resulting from the attenuation and imbalance created by the added external filter resistance. Table 9-1 provides the gain error factor and gain error for several resistor values.

$$\text{Equation 2:} Gain\ Error\ Factor = \frac{3000}{R_S + 3000}$$

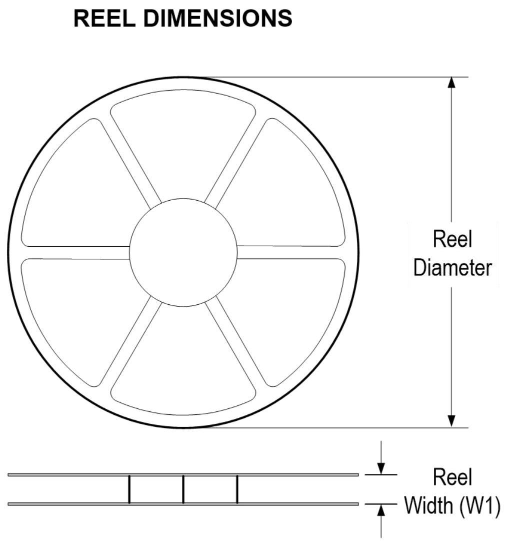
Where:

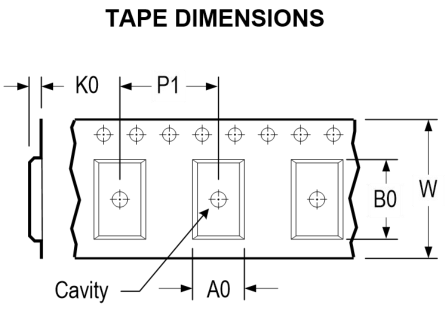
- RS is the external filter resistance value.

Gain Error Factor and Gain Error For External Input Resistors.

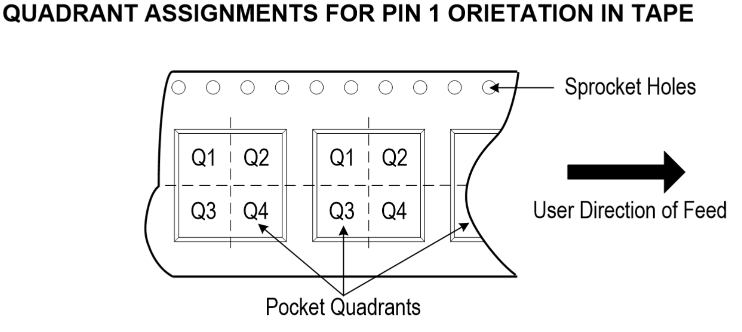
EXTERNAL RESISTANCE (Ω)	GAIN ERROR FACTOR	GAIN ERROR (%)
5	0.998	0.17
10	0.997	0.33
100	0.968	3.23

Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

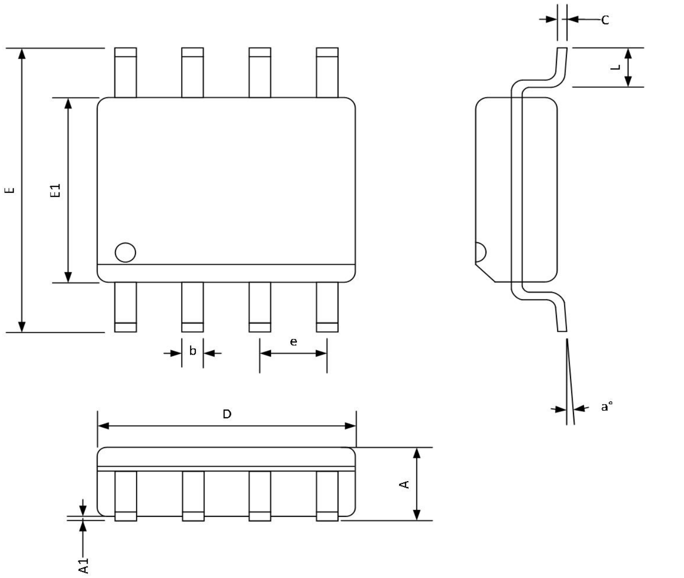


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA1240A2XS8/R8	SOIC	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1

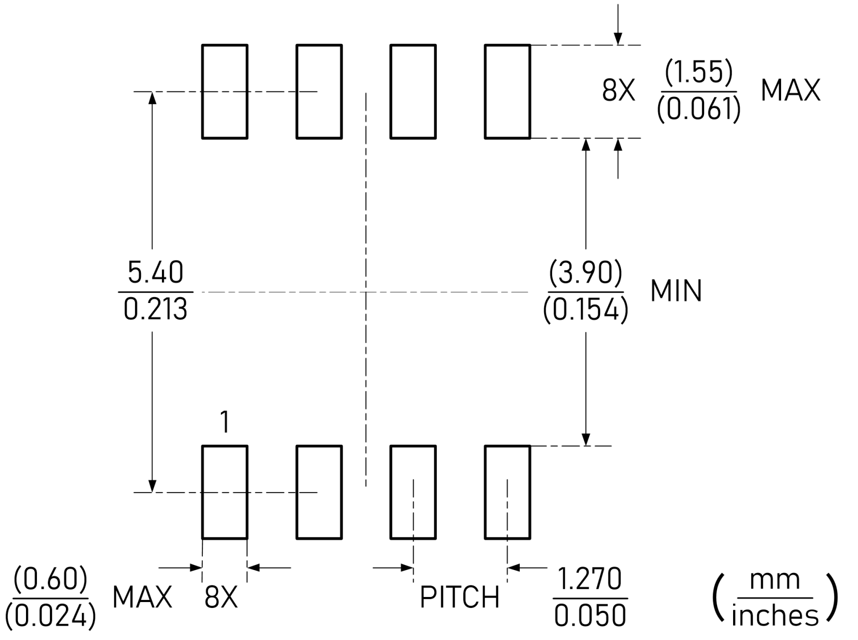
Package Dimension

DIMENSIONS, SOIC-8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.750
A1	0.070	--	0.230
b	0.306	--	0.506
c	0.190	--	0.250
D	4.700	4.900	5.100
E	5.800	6.000	6.200
E1	3.700	3.900	4.100
e	1.270TYP		
L	0.450	--	0.800
a°	0°	--	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



Important Notice

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