

General Description

The LTA180Q series of current sense amplifiers (also called current shunt monitors) are designed for cost-optimized applications, that sense voltage drops across current-sense resistors at common-mode voltages from -0.2 V to $+30\text{ V}$, independent of the supply voltage. The LTA180Q series integrate a matched resistor gain network in four fixed-gain device options: 20 V/V , 50 V/V , 100 V/V , or 200 V/V . This matched gain resistor network minimizes gain error and reduces the temperature drift.

The LTA180Q series operate from a single $+2.7\text{ V}$ to $+5.5\text{ V}$ power supply, drawing a maximum of $110\mu\text{A}$ of supply current. The device is specified from -40°C to $+125^\circ\text{C}$, and offered in SOT23-5L packages.

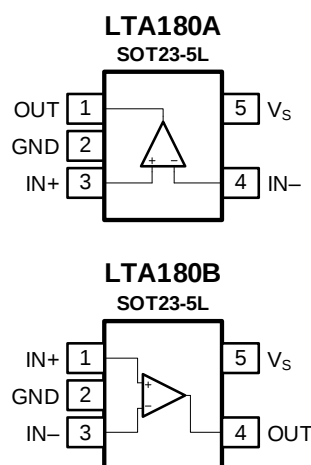
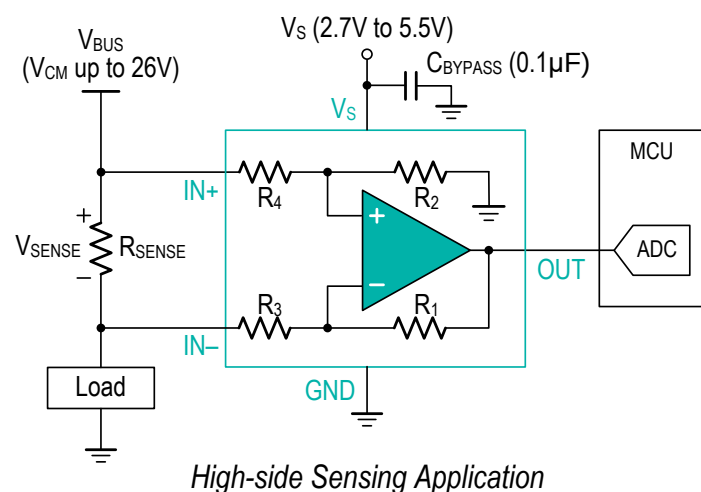
Features and Benefits

- Wide common-mode range: -0.2 V to 30 V
- Offset voltage
 - $\pm 150\mu\text{V}$ Maximum at $V_{\text{CM}} = 0\text{ V}$
 - $\pm 500\mu\text{V}$ Maximum at $V_{\text{CM}} = 12\text{ V}$
- Accuracy
 - Maximum $\pm 1\%$ Gain Error
 - Maximum $1\mu\text{V}/^\circ\text{C}$ Offset Drift
- Gains Options:
 - 20 V/V (LTA180A1Q Qualified, LTA180B1Q Compatible)
 - 50 V/V (LTA180A2Q Compatible, LTA180B2Q Compatible)
 - 100 V/V (LTA180A3Q Compatible, LTA180B3Q Compatible)
 - 200 V/V (LTA180A4Q Compatible, LTA180B4Q Compatible)
- Output slew rate: $1.3\text{ V}/\mu\text{s}$
- Quiescent Current: Maximum $230\mu\text{A}$
- Package: SOT23-5L
- Automotive Grade 1

Applications

- Motor Control
- Battery Monitor, BMS
- Power Management
- Lighting Control
- Over-Current Detection
- Solar Inverters

Block Diagram and Pin Configuration (Top View)



Pin Description

Symbol	Description
IN–	Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+	Current-sense amplifier positive input. For high-side applications, connect to bus-voltage (V_{BUS}) side of sense resistor. For low-side applications, connect to load side of sense resistor.
OUT	Output voltage. The voltage range extends to within millivolt of each supply rail.
V_S	Positive power supply. Typically, the voltage is from 2.7 V to 5.5 V. A bypass capacitor of 0.1 μ F as close to the part as possible should be used between power supply pin and ground pin.
GND	Negative power supply.

Ordering Information

Orderable Type Number	Gain (V/V)	Package Name	Package Quantity	Eco Class ⁽¹⁾	Marking Code
LTA180A1QT5/R6	20	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	8Q1
LTA180A2QT5/R6	50	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	8Q2
LTA180A3QT5/R6	100	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	8Q3
LTA180A4QT5/R6	200	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	8Q4
LTA180B1QT5/R6	20	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	8Q1
LTA180B2QT5/R6	50	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	8Q2
LTA180B3QT5/R6	100	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	8Q3
LTA180B4QT5/R6	200	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	8Q4

(1) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).

(2) Please contact to your Linearin representative for the latest availability information and product content details.

Limiting Value

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_S to GND	+10 V
Analog Inputs (IN+, IN–), Differential ($V_{IN+} - V_{IN-}$)	–30 V to +30 V
Analog Inputs (IN+, IN–), Common-Mode	(GND – 0.3V) to +30 V
Input Current Into All Pins	5 mA
Output	(GND – 0.3V) to ($V_S + 0.3V$)
Maximum output current, I_{OUT}	8 mA
Storage Temperature Range, T_{stg}	–65 °C to +150 °C
Junction Temperature, T_J	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9	± 4 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014	± 2 000	
	Machine model (MM), per JESD22-A115C	± 400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

$T_A = +25^\circ\text{C}$, $V_S = +5.0\text{V}$, $V_{IN+} = 12\text{V}$, and $V_{SENSE} = V_{IN+} - V_{IN-}$ unless otherwise noted.

Boldface limits apply over the specified temperature range, $T_A = -40$ to $+125^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
INPUT CHARACTERISTICS						
V _{OS}	Offset voltage	Referred-to-input		± 100	± 500	μV
		Referred-to-input, V _{IN+} = 0 V		± 25	± 150	
V _{OS} TC	Offset voltage drift	Referred-to-input, over Temperature		0.4	1	μV/°C
I _B	Input bias current	V _{SENSE} = 0 mV, V _{IN+} = 0 V		0.05		μA
		V _{SENSE} = 0 mV		40		
I _{OS}	Input offset current	V _{SENSE} = 0 mV		± 0.05		μA
V _{CM}	Common-mode input voltage range	Referred-to-input	-0.2		30	V
CMRR	Common-mode rejection ratio	V _{IN+} = 0 V to +26 V, V _{SENSE} = 10 mV, T _A = -40 to +125°C	84	100		dB
OUTPUT CHARACTERISTICS						
G	Gain	LTA180A1, LTA180B1		20		V/V
		LTA180A2, LTA180B2		50		
		LTA180A3, LTA180B3		100		
		LTA180A4, LTA180B4		200		
E _G	Gain error	V _{OUT} = 0.5V to V _S -0.5 V		± 0.1	± 1	%
E _G TC	Gain error drift	over Temperature		1.5	15	ppm/°C
	Nonlinearity Error	V _{OUT} = 0.5V to V _S -0.5 V		± 0.01		%
C _L	Maximum Capacitive Load	No sustained oscillation		1		nF
V _{OH}	Swing to V _S rail	R _L = 10kΩ to GND, T _A = -40 to +125°C		V _S -30		mV
V _{OL}	Swing to GND			V _{GND} +2		
DYNAMIC PERFORMANCE						
BW	Bandwidth	LTA180A1 and LTA180B1, C _L = 10pF		110		kHz
		LTA180A2 and LTA180B2, C _L = 10pF		80		
		LTA180A3 and LTA180B3, C _L = 10pF		30		
		LTA180A4 and LTA180B4, C _L = 10pF		14		
SR	Slew rate			1.5		V/μs
NOISE PERFORMANCE						
e _n	Voltage noise density	Referred-to-input		30		nV/√Hz
POWER SUPPLY						
V _S	Operating supply voltage		+2.7		+6	V
PSRR	Power supply rejection ratio	Referred-to-input, V _S = +2.7V to +5.5V, V _{SENSE} = 10 mV		± 4	± 20	μV/V
I _Q	Quiescent current	V _{SENSE} = 10 mV		180	250	μA
		over Temperature			290	
THERMAL CHARACTERISTICS						
T _A	Operating temperature		-40		+125	°C
θ _{JA}	Package Thermal Resistance	SOT23-5L		190		°C/W

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

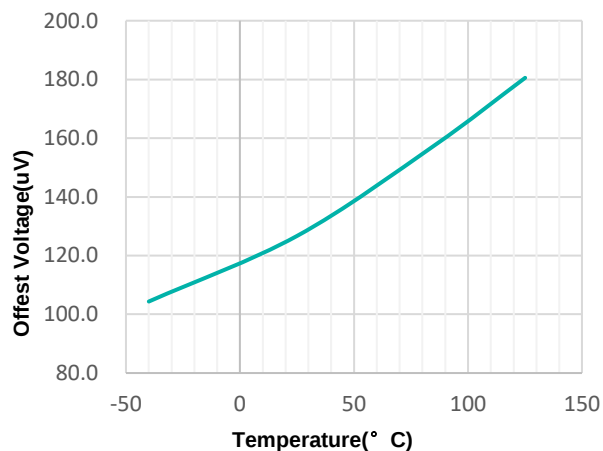
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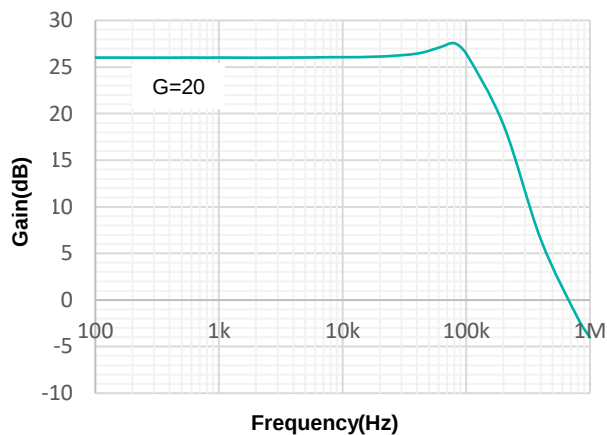
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Typical Performance Characteristics

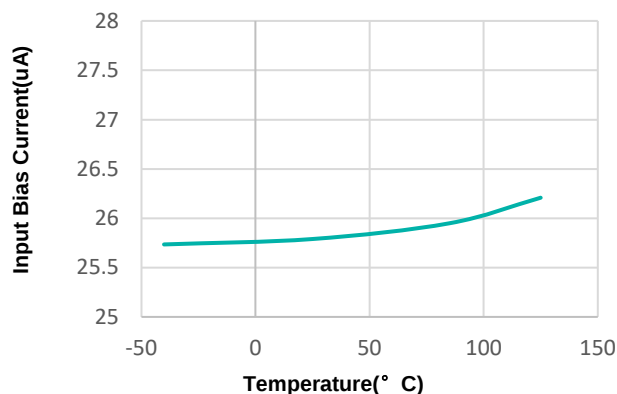
At $T_A = +25^\circ\text{C}$, $V_S = +5.0\text{V}$, and $V_{IN+} = 12\text{V}$, unless otherwise noted.



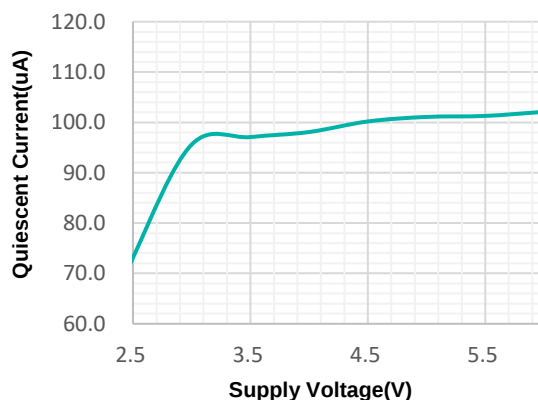
Offset Voltage vs. Temperature



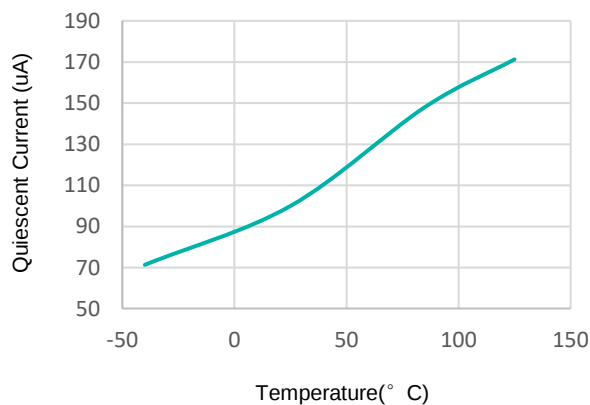
Gain vs. Frequency



Input Bias Current vs. Temperature



Quiescent Current vs. Supply Voltage



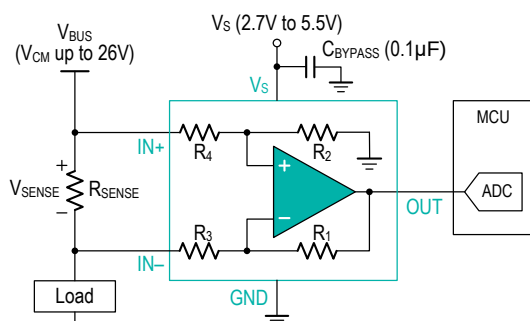
Quiescent Current vs. Temperature

Application Notes

BASIC CONNECTIONS

Figure 1 shows the basic connections for the LTA180 series. The input pins, IN+ and IN-, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.



High-side Sensing Application
Figure 1. Typical Application

POWER SUPPLY

The input circuitry of the LTA180 can accurately measure beyond its power-supply voltage, V_S . For example, the V_S power supply can be 5V, whereas the load power-supply voltage can be from 2.7V to 5.5V. However, the output voltage range of the OUT terminal is limited by the voltages on the power-supply pin. Note also that the LTA180 can withstand the full $-0.2V$ to $+30V$ range in the input pins, regardless of whether the device has power applied or not.

PRECISE LOW-SIDE CURRENT SENSING

When used in low-side current sensing applications, the offset voltage of the LTA180 series is within $\pm 150\mu V$. The low offset performance of the LTA180 has several benefits. First, the low offset allows the device to be used in applications that must measure current over a wide dynamic range. In this case, the low offset improves the accuracy when the sensed currents are on the low end of the measurement range. Another advantage of low offset is the ability to sense lower voltage drop across the sense resistor accurately, thus allowing a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current sense circuit, and help improve the power efficiency of the end application.

The gain error of the LTA180 series is specified to be within 1% of the actual value. As the sensed voltage becomes much larger than the offset voltage, this voltage becomes the dominant source of error in the current sense measurement.

INPUT DIFFERENTIAL OVERLOAD

If the differential input voltage ($V_{IN+} - V_{IN-}$) times gain exceeds the voltage swing specification, the LTA180 series drive the output as close as possible to the positive supply,

and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the LTA180 series return to the expected value approximately $20\mu s$ after the fault condition is removed. When the LTA180 output is driven to either the supply rail or ground, increasing the differential input voltage does not damage the device as long as the absolute maximum ratings are not violated. Following these guidelines, the LTA180 maintains polarity, and does not suffer from phase reversal.

INPUT FILTERING

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the $\pm 30\%$ tolerance of the internal resistances. Figure 2 shows a filter placed at the inputs pins.

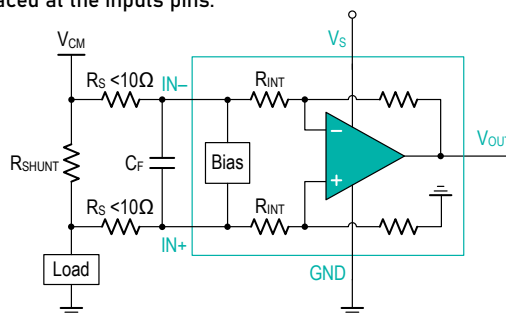


Figure 2. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors should be kept to 10Ω or less if possible to reduce impact to accuracy. The internal bias network shown in Figure 2 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the

Application Notes (continued)

voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistor add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R_{INT} as shown in Figure 2. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in Equation 1:

$$\text{Gain Error Factor} = \frac{1250 \times R_{INT}}{1250 \times R_S + 1250 \times R_{INT} + R_S \times R_{INT}}$$

where:

R_{INT} is the internal input resistor (R3 and R4, 10k Ω), and R_S is the external series resistance.

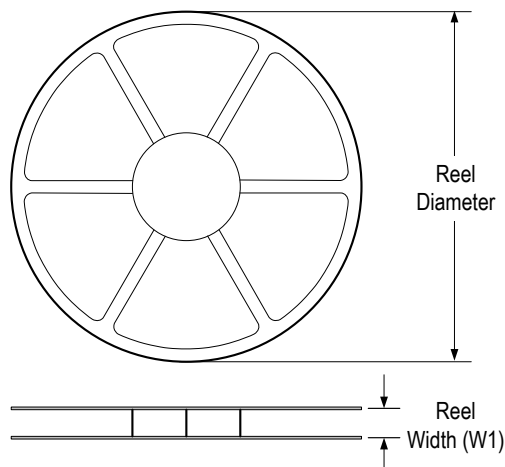
The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor})$$

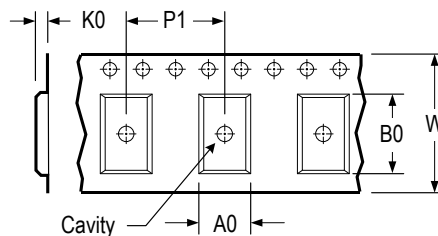
For LTA180, a series resistance of 10 Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 0.89% solely because of the external 10 Ω series resistors.

Tape and Reel Information

REEL DIMENSIONS

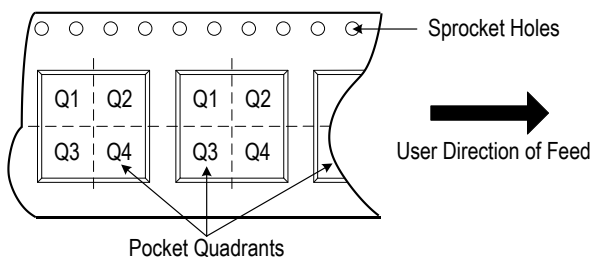


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

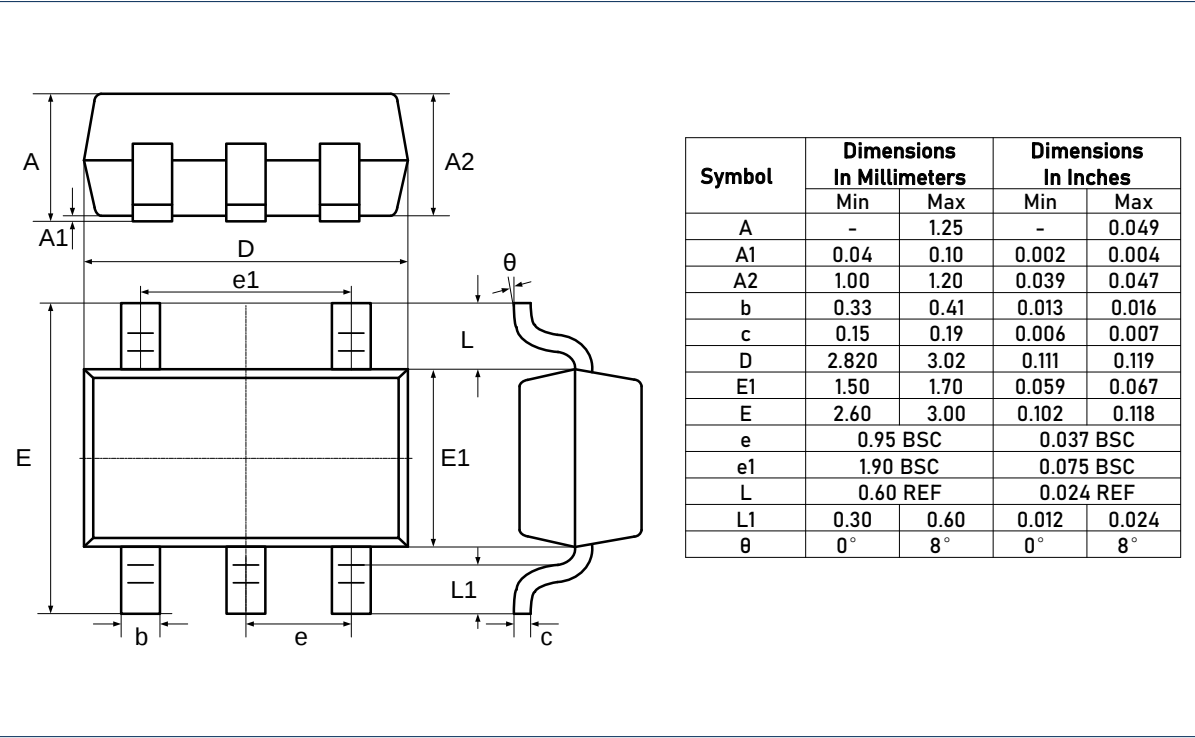


* All dimensions are nominal

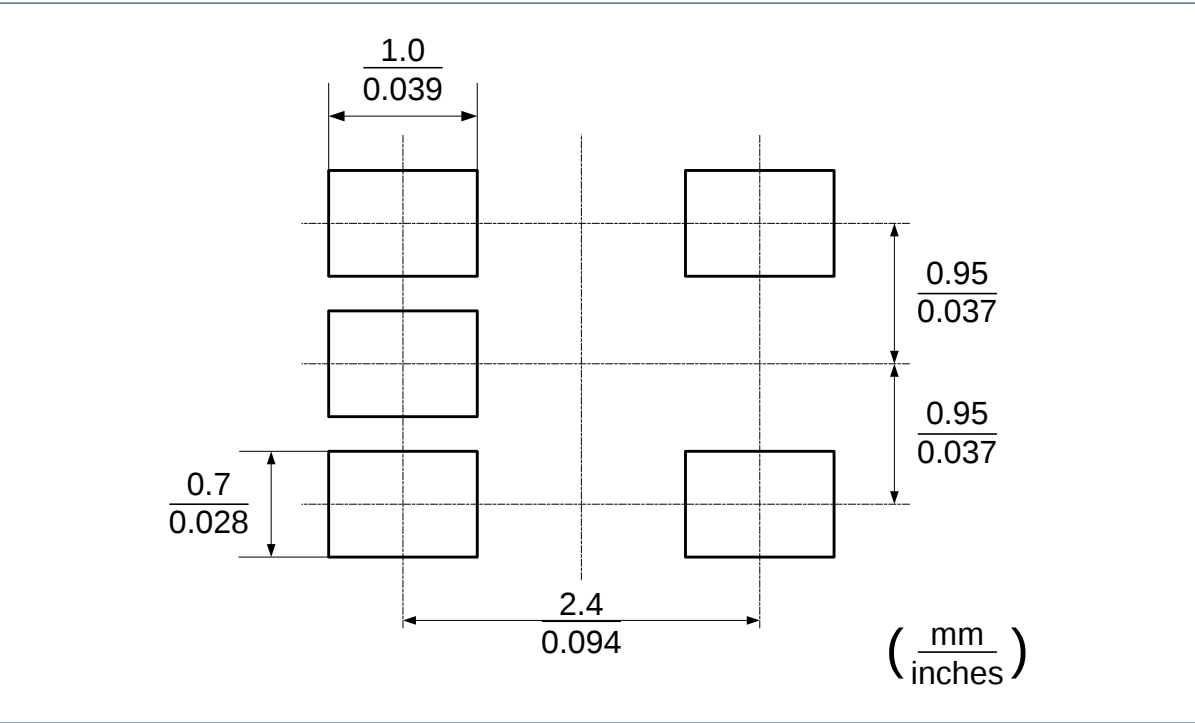
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA180A1QT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA180A2QT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA180A3QT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA180A4QT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA180B1QT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA180B2QT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA180B3QT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA180B4QT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

Package Outlines

DIMENSIONS, SOT23-5L



RECOMMENDED SOLDERING FOOTPRINT, SOT23-5



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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IMPORTANT NOTICE

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