LTM5030/LTM5032
Low-Voltage H-Bridge Driver

General Description

The LTM5030/LTM5032 offers an integrated motor driver solution for cameras, consumer electronics, toys, and other low-voltage or battery-powered motion control applications. This device is capable of driving a DC motor or other actuators such as solenoids. The output driver stage comprises n-channel power MOSFETs configured in an H-bridge topology to drive the motor winding. An integrated charge pump generates the necessary gate drive voltage.

The LTM5030/LTM5032 can deliver a peak output current of up to 1.6A. It supports a motor supply voltage range of 0 to 11V and a logic supply voltage range of 1.65V to 7.0V.

The LTM5030/LTM5032 features a PWM (IN1/IN2) input interface, while the LTM5032 is equipped with a PH/EN input interface, both of which are compatible with industry-standard devices.

The LTM5030/LTM5032 incorporates an ultra-low-power standby mode with a quiescent current consumption of 40nA. It also integrates internal protection features including over current protection, short-circuit protection, undervoltage lockout, and thermal shutdown.

Features And Benefits

- Independent motor and logic power supply pins:
  - Motor VM: 0 to 11V
  - Logic VCC: 1.65 to 7V
- Low on-resistance, high-side + low-side (HS + LS) 440mΩ;
- N SLEEP pin;
- Low-power sleep mode (40nA);
- Maximum drive current of 1.6A;
- Pulse width modulation (PWM) or PH/EN interface:
  - LTM5030: PWM, IN1/IN2 control
  - LTM5032: PH/EN control
- Comprehensive fault protection features include:
  - VCC under-voltage protection (UVP)
  - Over-current protection (OCP)
  - Built-in thermal shutdown protection (TSD）

Application

- Cameras
- Consumer Products
- Toys
- Robotics
- Office Equipment

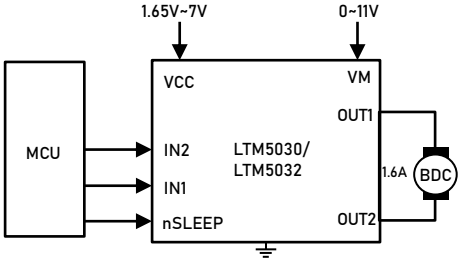


Table of Content

Ordering Information [1]

Part Number	Package Type	Package Size	Package Quantity	ECO Class [2]	Mark Code
LTM5030EYS8/R8	ESOP-8L	4.90mm*3.92mm	Tape and Reel,4000	Green (RoHS & no Sb/Br)	MA30
LTM5032EYS8/R8	ESOP-8L	4.90mm*3.92mm	Tape and Reel,4000	Green (RoHS & no Sb/Br)	MA32
LTM5030YF8/R6	DFN2x2-8L	2.0mm*2.0mm	Tape and Reel,3000	Green (RoHS & no Sb/Br)	MA30
LTM5032YF8/R6	DFN2x2-8L	2.0mm*2.0mm	Tape and Reel,3000	Green (RoHS & no Sb/Br)	MA32

(1) Please contact to your Linearin representative for the latest availability information and product content details.

(2) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free)

Pin Description (Top View)

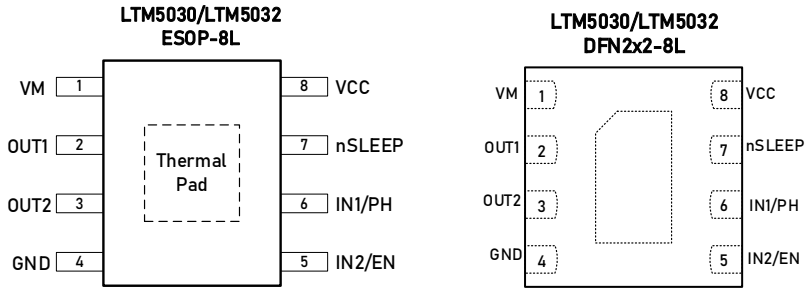


Figure 1 Pinout Diagram

Pin name	Pin	Functional description
VM	1	Motor power supply.Bypass to ground with 0.1μF ceramic capacitor
OUT1	2	H-bridge output1,connected to OUT2 via load.
OUT2	3	H-bridge output2, connected to OUT1 via load.
GND	4	Ground.
IN2/EN	5	Input signal 2, with internal pull-down resistor.
IN1/PH	6	Input signal 1, with internal pull-down resistor
nSLEEP	7	Sleep mode input pin. Integrated with internal pull-down resistor. A logic low level input triggers the chip into low-power sleep mode, while a high level input activates normal operational mode.
VCC	8	For logic circuit power supply, bypass to ground using a 0.1μF ceramiccapacitor.

Limiting Value

Parameter	Absolute Maximum Rating
Motorpower supply VM voltage range	12V
Operating Voltage Range for Logic Circuits	7V
Input logic voltage range	7V
Peak drive current of OUT1 and OUT2.	1.6A
Storage Temperature Range,Tstg	−40℃ to +85℃
Junction Temperature, TJ	150℃
LeadTemperatureRange(Soldering10sec)	260℃

ESD Ratings

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V

Thermal Information

Thermal Metric		Package	Level	Unit
θ_{JA}	Package Thermal Resistance	DFN2x2-6L	95	℃/W
		ESOP-8L	63	

Electrical Characteristics (T_A=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
General Parameters						
VM Operating Voltage Range	VM		0		11	V
VCC Operating Voltage Range	VCC		1.65		7	V
VM Operating Current	I_{VM}	VM=5V, VCC=3V, f_{PWM}=0		50	100	μA
		VM=5V, VCC=3V, f_{PWM}=50 kHz		0.3	1.0	mA
VM sleep-mode current	I_{VMQ}	VM=5V, VCC=3V, nSLEEP=0		4	20	nA
VCC Operating Current	I_{CC}	VM=5V, VCC=3V, f_{PWM}=0		500	800	μA
		VM=5V, VCC=3V, f_{PWM}=50 kHz		400	1000	μA
VCC Standby Current	I_{CCQ}	VM=5V, VCC=3V, nSLEEP =0		4	20	μA
Logical input parameters(IN1，PH, IN2，EN, nSLEEP)						
Logic input high voltage	$V_{IN(1)/PH}$			0.46*VCC	0.5*VCC	V
Logic input LOW voltage	$V_{IN(2)/EN}$		0.25*VCC	0.38*VCC		V
Input hysteresis of logical signals	V_{HYS}			0.08*VCC		V
Logical Input Current	$I_{IN(1)/PH}$	V_{IN} =3.3V			50	μA
	$V_{IN(2)/EN}$	V_{IN}=0V	-5		5	μA
Input pull-down resistor	R_{PD}			100		kΩ
		nSLEEP foot postion		55		kΩ
Motor Drive Parameters						
RDS(on)Upper tube+Lower tube	$R_{DS(on)}$	I_{OUT}=800mA,VM=5V, VCC=3V T_J=25°C		440	480	mΩ
Shutdown Leakage Current	I_{off}	VOUT=0	-200		200	nA
Protective Circuit Parameters						
Under-Voltage Protection Threshold for VCC	V_{UVLO}	V_{BB} increasing			1.7	V
Under Voltage Protection Lockout (UVLO)	$V_{UVLOhys}$			0.1		mV
Overcurrent protection current threshold	I_{OCP}		1.9		5.5	A
Overcurrent Protection Hysteresis Filtering Time	T_{DEG}			2		μs
Overcurrent Protection Retry Interval	T_{RETRY}			2		ms
Thermal protection operating temperature	T_{JTSD}	Temperature Increasing	150	160	180	°C
Thermal shutdown hysteresis	T_{TSDhys}	Recovery=T_{JTSD}–T_{TSDhys}		15		°C

Function Diagram

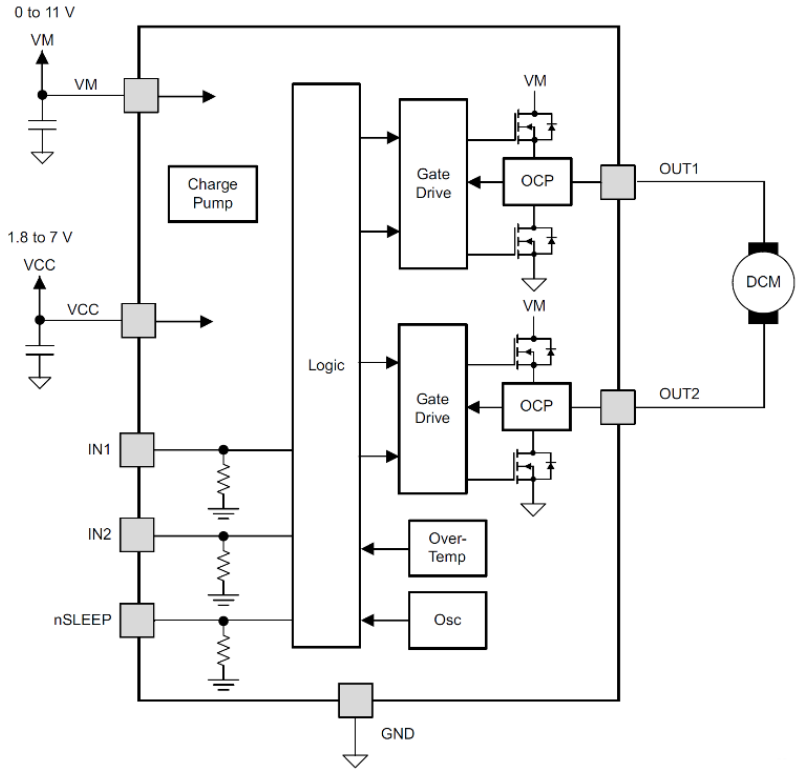


Figure 2 LTM5030 Functional Block Diagram

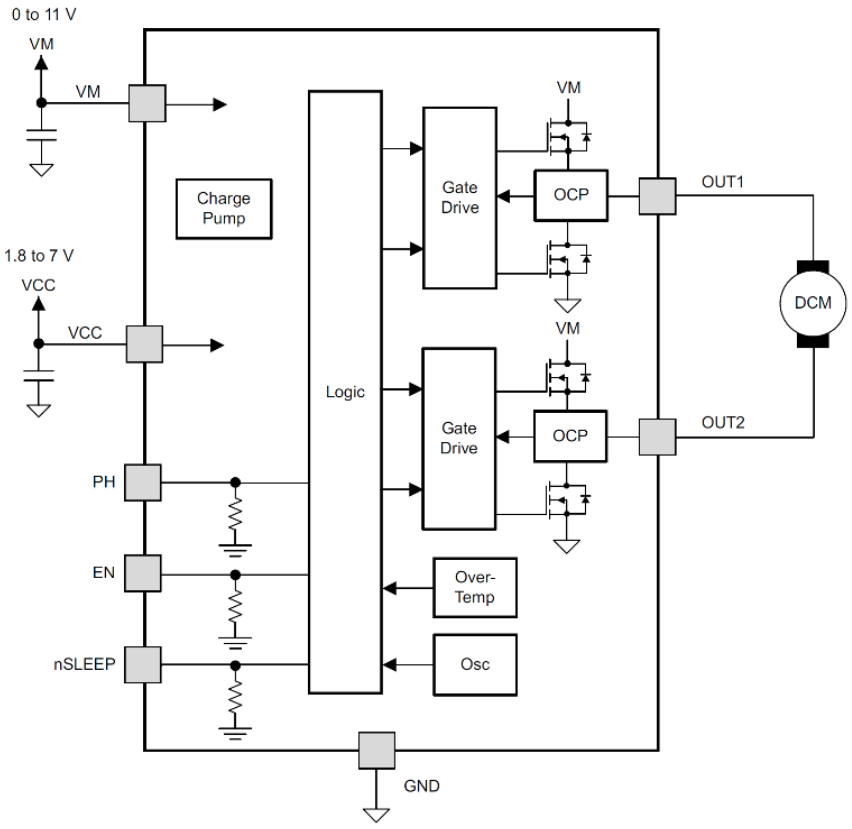


Figure 3 LTM5032 Functional Block Diagram

Control Timing

Order Number	Symbol	Test Condition	Min	Max	Unit
1	t1	Delay time, high PH to low OUT1		400	ns
2	t2	Delay time, PH high to OUT2 high		200	ns
3	t3	Delay time, low PH to high OUT1		200	ns
4	t4	Delay time, low PH to OUT2 low		400	ns
5	t5	The delay time is higher when EN is high than when OUTx is high.		200	ns
6	t6	The delay time is lower than the OUTx level.		160	ns
7	t7	Output enable time		100	ns
8	t8	Output close time		100	ns
9	t9	The delay time is INX higher than OUTx		120	ns
10	t10	The delay time is lower at INx than at OUTx		120	ns
11	t11	Output rise time	30	188	ns
12	t12	Output fall time	30	188	ns
13	TWAKE	Wake-up time, nSLEEP rising edge to chip operation		10	µs

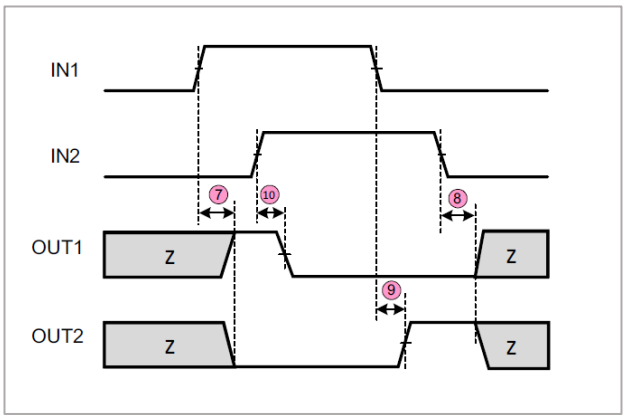


Figure 4 Timing Diagram1

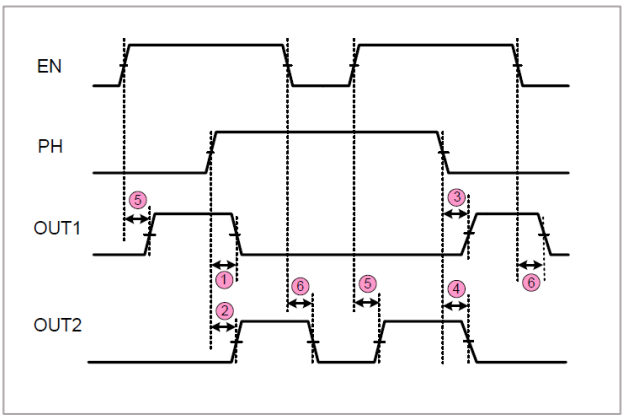


Figure 5 Timing Diagram2

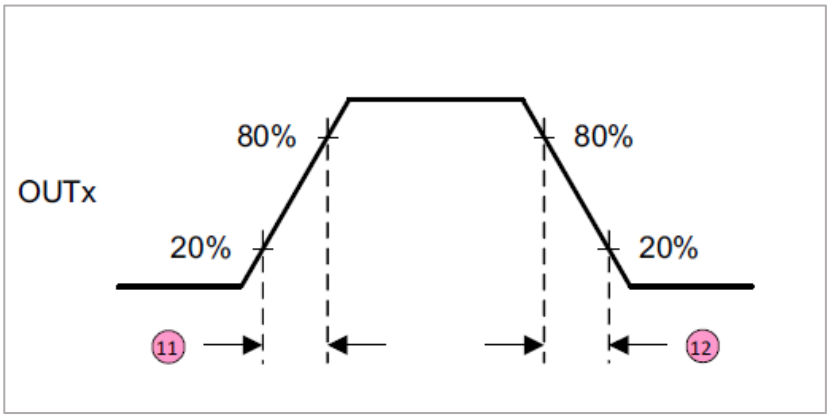


Figure 6 Timing Diagram3

Functional Description

The LTM5030 is an H-bridge driver designed to power DC motors or other devices like solenoids. Its output is controlled via the PWM interface (IN1/IN2) on the LTM5030 or the PH/EN interface on the LTM5032. The chip features a low-power sleep mode that can be activated using the nSLEEP pin. It integrates FET drivers and control circuits, significantly reducing the number of components in the motor drive system. Additionally, the LTM5030/LTM5032 incorporates protection features including under-voltage lockout, overcurrent protection, and thermal shutdown.

H bridge Control Mode

The LTM5030 is controlled via PWM input interfaces (IN1/IN2), with each output controlled by its corresponding input pin as shown in the table below.

nSLEEP	IN1	IN2	OUT1	OUT2	Function
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reversal
1	1	0	H	L	Forward
1	1	1	L	L	Braking (slow decay)

The LTM5032 is controlled via the PHASE/ENABLE interface, which uses the PH pin to control the H-bridge current direction and the EN pin to enable or disable the H-bridge, as shown in the table below:

nSLEEP	PH	EN	OUT1	OUT2	Slow Attenuation
0	X	X	Z	Z	Coast
1	X	0	L	L	Braking (slow decay)
1	1	1	L	H	Reversal
1	0	1	H	L	Forward

Low Power Sleep Mode

When the nSLEEP pin is at a low logic level, the LTM5030/LTM5032 enters a low-power sleep mode. In this state, all unnecessary internal circuits are disabled, minimizing power consumption.

Power Supply And Input Terminals

The input pins can operate within their recommended range with or without VCC/VM power supply, ensuring no leakage current path exists. Each input pin is equipped with a weak pull-down resistor (approximately 100 kΩ) to ground.

VCC and VM can be powered on and off in any sequence. When VCC is turned off, the device enters a low-power state and draws minimal current from VM. When the logic power supply voltage ranges between 1.65V and 7V, VCC and VM can be connected together

The VM voltage lacks any undervoltage lockout protection (UVLO), so the internal device logic remains active as long as VCC exceeds 1.65V. While the VM pin voltage may drop to 0V, the load might not operate effectively at low VM voltages.

VCC Under-Voltage Lockout Protection

When the VCC voltage falls below the under-voltage lockout threshold, all field-effect transistors in the h-bridge will be disabled. Operation resumes once VCC exceeds the UVLO threshold.

Overcurrent Protection

The analog current-limiting circuit on each FET restricts current flow by deactivating the gate driver. If this analog current limit persists beyond tDEG, all FETs in the H-bridge will be disabled and automatically resume operation after the tRETRY delay. Overcurrent is detected on both high-side and low-side FETs. Short circuits to VM, GND, or between OUT1 and OUT2 will trigger overcurrent protection.

Overtemperature Shutdown

If the chip temperature exceeds the safety threshold, all FETs in the H-bridge will be turned off. Once the temperature returns to the safe range, the driver will automatically resume operation.

Exceedingly	Condition of Occurrence	H Bridge State	Exit Exception Condition
VCC Undervoltage (UVLO) Protection	VCC<1.6V	Fully Off	VCC>1.65V
Overcurrent Protection (OCP)	I_{OUT}>1.9A(MIN)	Fully Off	Delayed t_{REETRY}
Overtemperature Shutdown (TSD)	TJ>150℃(MIN)	Fully Off	TJ>140℃

Operate Mode

The LTM5030/LTM5032 operates normally unless the nSLEEP pin is low. In sleep mode, the H-bridge FET is turned off in Hi-Z state. If nSLEEP is set high, the LP733x automatically exits sleep mode. Under fault modes such as under-voltage protection lockout, overcurrent protection, and over-temperature shutdown, the H-bridge output is disabled.

Work Pattern	Condition of Occurrence	H Bridge State
regular work	nSLEEP = 1	drive
dormancy mode	nSLEEP = 0	fully off
fault-pattern	UVLO, OCP, TSD	fully off

Typical Application Diagram

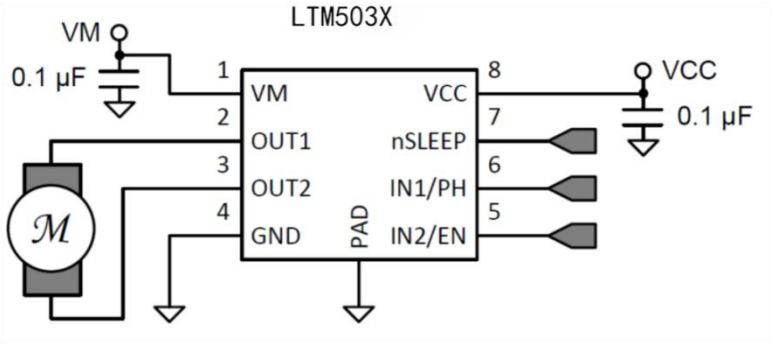


Figure 7 Mixed Decay Chopper Drive

Typical Working Conditions

Parameter	Symbol	Numerical
Motor Power Supply	VM	9V
Logic Circuit Poweer Supply	VCC	3.3V
Drive Current	I_{OUT}	800mA

Power Consumption

The LTM5030/LTM5032's self-power consumption is primarily determined by the on-resistance $R_{DS(ON)}$ of its output FET. The average self-power consumption during stepper motor operation can be approximated as:

$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$

P_{TOT} is the total self-power consumption of the chip.

$R_{DS\,(ON)}$ is the sum of the on-resistances of the FETs on and off the chip.

$I_{OUT\,(RMS)}$ is the RMS or DC output current supplied to the load.

The maximum self-dissipated power a chip can handle depends on the ambient temperature and heat dissipation conditions. Note that $R_{DS(ON)}$ increases with rising temperature, so when the chip heats up, its self-power consumption also rises.

The LTM5030/LTM5032 features thermal shutdown protection. When the chip temperature exceeds approximately 150°C, its H-bridge will be disabled until the temperature returns to a safe range. This thermal shutdown occurs when the chip experiences excessive power dissipation, inadequate heat dissipation, or high ambient temperature.

Waveform Example

Figure 8 Reverse, 50% blank

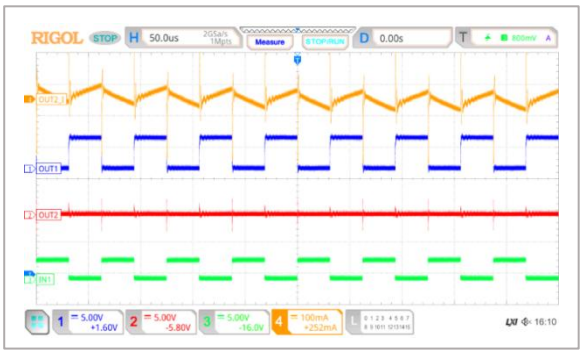


Figure 9 Positive, 50% blank

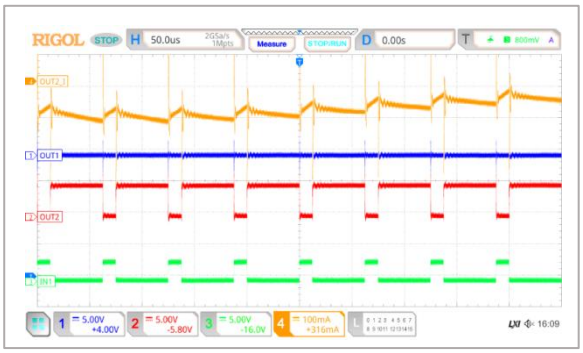


Figure 10 Reverse, 50% blank

Figure 11 Positive, 50% blank

Recommended Working Power Supply

VCC and VM can be powered on and off in any sequence. When VCC is turned off, the device enters a low-power state and draws minimal current from VM. When the logic power supply voltage ranges between 1.65 and 7 volts, VCC and VM can be connected together.

Connect the 0.1µF ceramic capacitors to ground via the VM and VCC pins, and position these capacitors as close as possible to the VM and VCC pins.

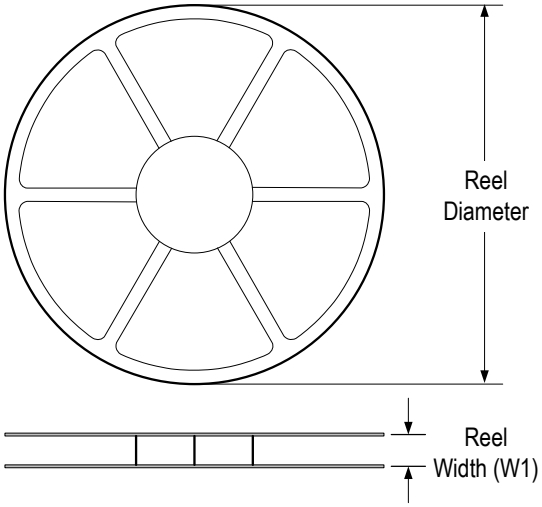
The VM power supply lacks under-voltage lockout protection. As long as VCC remains above 1.65V, the chip's internal logic circuit will continue to operate. This means the VM pin voltage may drop to 0V, but if the VM voltage becomes too low, the load might not be fully driven.

PCB Layout

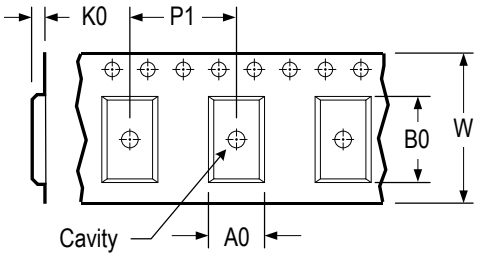
VM and VCC terminals should be grounded with low-impedance ceramic bypass capacitors, preferably rated at 0.1µF. These capacitors should be placed as close as possible to the VM and VCC pins and connected to the device's GND pin via a thick trace or ground plane.

Tape and Reel Information

REEL DIMENSIONS

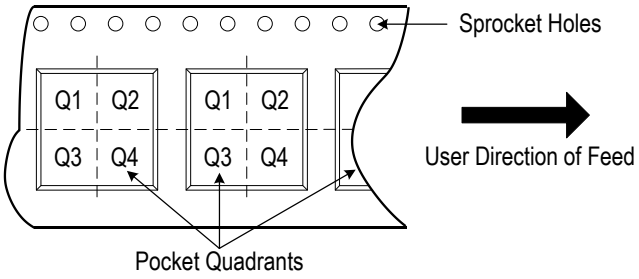


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

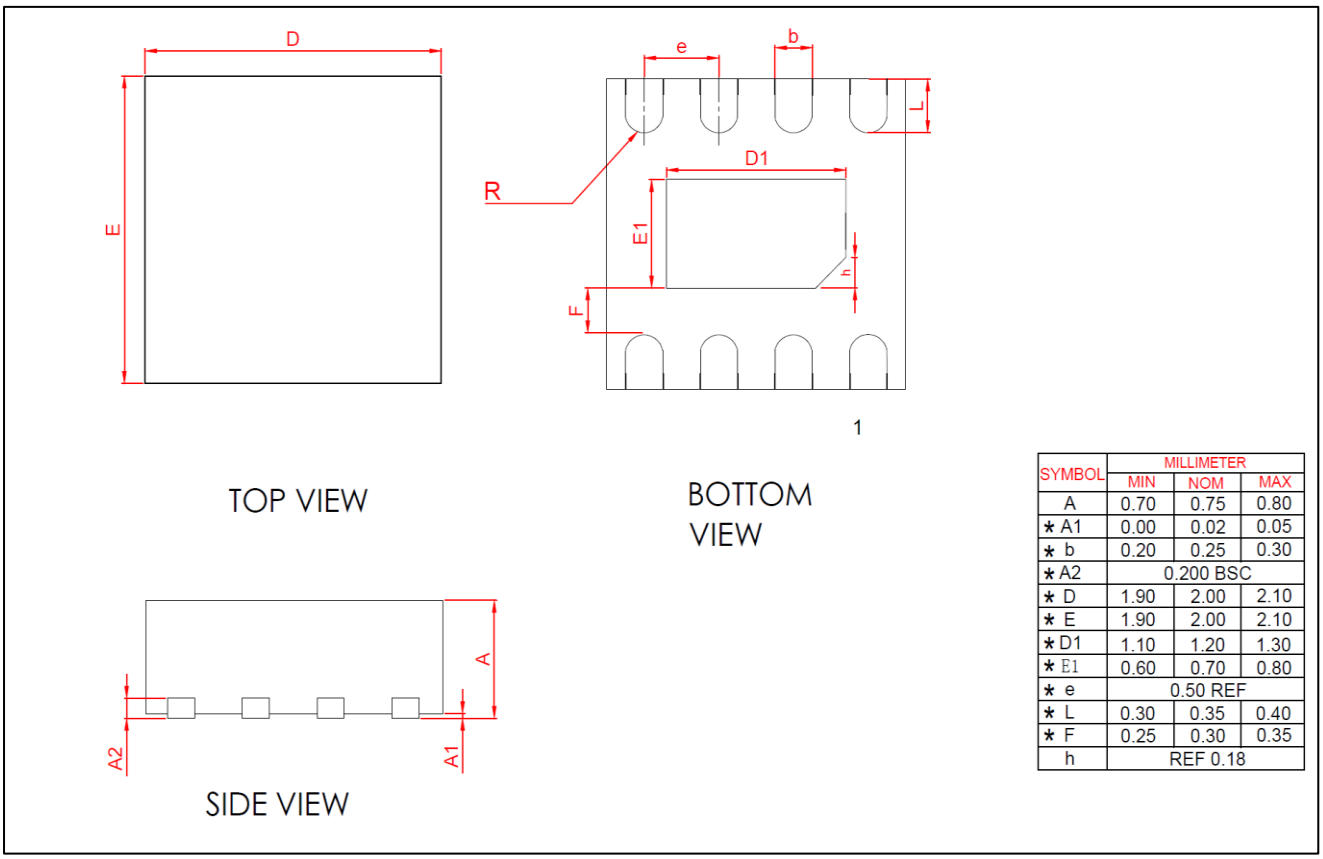


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTM5030EYS8/R8	ESOP	8	4000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTM5032EYS8/R8	ESOP	8	4000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTM5030YF8/R6	DFN2x2	8	3000	178	9.5	2.25	2.25	1.0	4.0	8.0	Q1
LTM5032YF8/R6	DFN2x2	8	3000	178	9.5	2.25	2.25	1.0	4.0	8.0	Q1

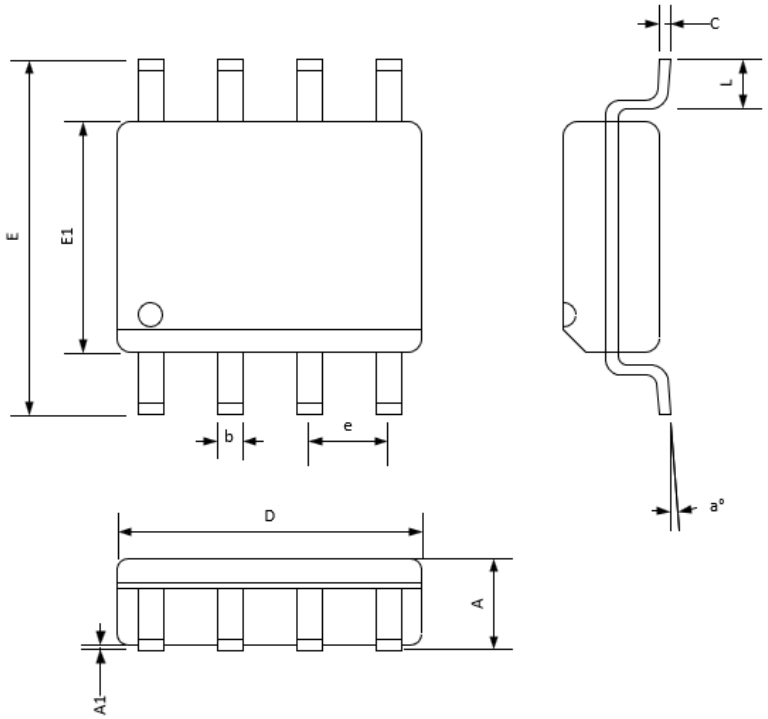
Package Outlines

DFN2x2-8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
⋆ A1	0.00	0.02	0.05
⋆ b	0.20	0.25	0.30
⋆ A2		0.200 BSC	
⋆ D	1.90	2.00	2.10
⋆ E	1.90	2.00	2.10
⋆ D1	1.10	1.20	1.30
⋆ E1	0.60	0.70	0.80
⋆ e		0.50 REF	
⋆ L	0.30	0.35	0.40
⋆ F	0.25	0.30	0.35
h		REF 0.18	

ESOP-8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.75
A1	0.10	--	0.23
b	0.35	--	0.48
c	0.19	--	0.25
D	4.70	4.90	5.00
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	--	0.80
a°	0°	--	8°

Important Notice

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