LTLB0104

4-Bit Bi-Directional, Level-Shifting, Voltage Translator

General Description

This device is a 4-bit non-inverting level translator which uses two separate configurable power-supply rails. The A port tracks the V_{CCA} pin supply voltage. The V_{CCA} pin accepts any supply voltage between 1.4V and 3.6V. The B port tracks the V_{CCB} pin supply voltage. The V_{CCB} pin accepts any supply voltage between 1.65V and 5.5V. Two input supply pins allow for low voltage bidirectional translation between any of the 1.5V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance (Hi-Z) state.

To put the device in the Hi-Z state during power-up or power-down periods, tie OE to GND through a pulldown resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

Features

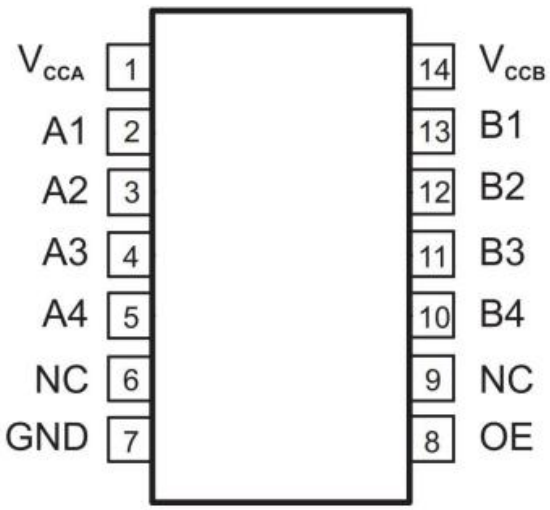
- No direction-control signal needed
- Maximum data rates:
  - 110Mbps (push pull)
  - 1.2Mbps (open drain)
- 1.4V to 3.6V on A port and 1.65V to 5.5V on B port($V_{CCA} \leq V_{CCB}$)
- No Power-Supply Sequencing required - either V_{CCA} or V_{CCB} can be ramped first
- ESD protection:
  - HBM: 2kV for A port
  - HBM: 6kV for B port

Applications

- Handsets
- Smartphones
- Tablets
- Desktop PCs

Pin Description (Top View)

LTLB0104
TSSOP-14L



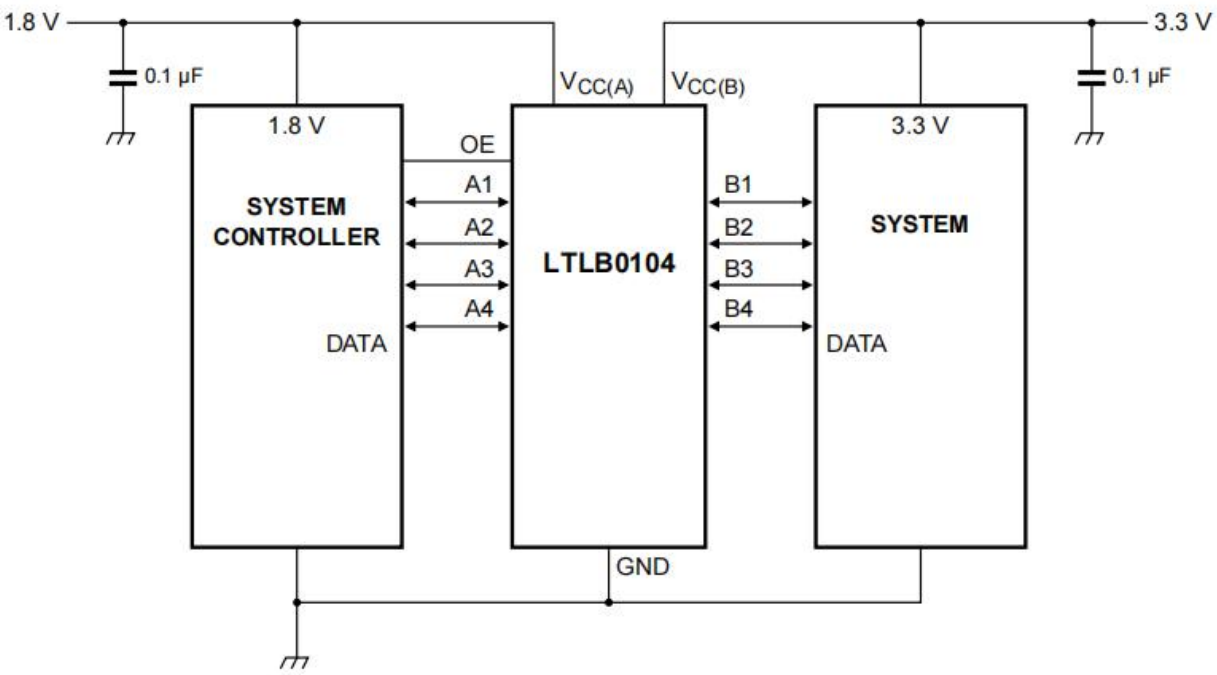
Pin Function

Symbol	Package Pin	Function
$V_{CC\ A}$	1	A-port supply voltage. 1.4 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
A1	2	Data input or output (referenced to $V_{CC(A)}$).
A2	3	Data input or output (referenced to $V_{CC(A)}$).
A3	4	Data input or output (referenced to $V_{CC(A)}$).
A4	5	Data input or output (referenced to $V_{CC(A)}$).
NC	6	No connection. Not internally connected.
GND	7	Ground.
OE	8	Tri-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
NC	9	No connection. Not internally connected.
B4	10	Data input or output (referenced to $V_{CC(B)}$).
B3	11	Data input or output (referenced to $V_{CC(B)}$).
B2	12	Data input or output (referenced to $V_{CC(B)}$).
B1	13	Data input or output (referenced to $V_{CC(B)}$).
$V_{CC\ B}$	14	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V.

Ordering Information

Package Type	Part Number	Quantity	Mark Code
TSSOP-14L	LTLB0104YT14/R6	Tape and Reel, 3 000	B104

Typical Application Circuit



Ordering Information

Parameter	Level	Unit
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	2 000	V
Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	1 000	

Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
V_{CCA}	Supply Voltage V_{CCA}	-0.5	4.6	V
V_{CCB}	Supply Voltage V_{CCB}	-0.5	6.5	V
V_{IA}	Input voltage, A Port	-0.5	4.6	V
V_{IB}	Input voltage, B Port	-0.5	6.5	V
V_{OA}	Voltage applied to any output in the high-impedance or power-off state,A Port	-0.5	4.6	V
V_{OB}	Voltage applied to any output in the high-impedance or power-off state,B Port	-0.5	6.5	V
V_{OA}	Voltage applied to any output in the high or low state, A Port	-0.5	V_{CCA}+0.5	V
V_{OB}	Voltage applied to any output in the high or low state, B Port	-0.5	V_{CCB}+0.5	V
I_{IK}	Input clamp current,V_I < 0	-50		mA
I_{OK}	Output clamp current,V_O < 0		-50	mA
I_O	Continuous output current	-50	50	mA
I_O	Continuous current through V_{CCA}, V_{CCB}, or GND	-100	100	mA
T_J	Junction temperature		+150	℃
T_{STG}	Storage Temperature	-65	+150	℃

Recommended Operating Conditions

Parameter	Description	Min	Max	Unit
V_{CCA}	Supply Voltage	1.4	3.6	V
V_{CCB}	Supply Voltage	1.65	5.5	V
T_A	Operating Temperature	-40	+85	℃

Electrical Characteristics

All typical value are at T_A =25°C unless otherwise specified.

Parameter	Descriptions	Conditions	V_{CCA}(V)	V_{CCB}(V)	T_A= 25°C			Unit
					Min.	Typ.	Max.	
V_{OHA}	Port A output high voltage	I_{OH} = –20µA, $V_{IB} \geq$ 0.15V	1.4	1.65 to 5.5	V_{CCA} x0.67			V
V_{OLA}	Port A output low voltage	I_{OL} = 180µA, $V_{IB} \leq$ 0.15V	1.4					V
V_{OHB}	Port B output high voltage	I_{OH} = –20µA, $V_{IA} \geq V_{CCA}$ – 0.2V	1.4	1.65 to 5.5	V_{CCB} x0.67			V
V_{OLB}	Port B output low voltage	I_{OL} = 220µA, $V_{IA} \leq$ 0.15V	1.4 to 5.5	1.65				V
I_I	Input leakage current	OE: $V_I = V_{CCI}$ or GND	1.4	1.65 to 5.5	-1		1	µA
I_{OZ}	High-impedance state output current	A or B port	1.4	1.65 to 5.5	-1		1	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_O$ = Open I_O = 0	1.4	1.65 to 5.5		1.5		µA
I_{CCA}	V_{CCA} supply current	$V_I = V_O$ = Open I_O = 0	3.6	0				µA
I_{CCA}	V_{CCA} supply current	$V_I = V_O$ = Open I_O = 0	0	5.5				µA
I_{CCA}	V_{CCA} supply current	$V_I = V_O$ = Open I_O = 0	1.5 to 3.6	2.3 to 5.5				µA
I_{CCB}	V_{CCB} supply current	$V_I = V_O$ = Open I_O = 0	1.4	1.65 to 5.5		1.5		µA
I_{CCB}	V_{CCB} supply current	$V_I = V_O$ = Open I_O = 0	1.5 to 3.6	2.3 to 5.5				µA
I_{CCB}	V_{CCB} supply current	$V_I = V_O$ = Open I_O = 0	3.6	0				µA
I_{CCB}	V_{CCB} supply current	$V_I = V_O$ = Open I_O = 0	0	5.5				µA
$I_{CCA}+I_{CCB}$	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0	1.4	2.3 to 5.5		3		µA
$I_{CCA}+I_{CCB}$	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0	1.5 to 3.6	2.3 to 5.5				µA
I_{CCZA}	High-impedance state V_{CCA} supply current	$V_I = V_O$ = Open, O = 0, OE = GND	1.4	1.65 to 5.5		0.05		µA
I_{CCZB}	High-impedance state V_{CCB} supply current	$V_I = V_O$ = Open, O = 0, OE = GND	1.4	1.65 to 5.5		4		µA
C_i	Input capacitance	OE	3.3	1.65 to 3.3		4		pF
C_{io}	Input-to-output internal capacitance	A port	3.3	1.65 to 3.3		6		pF
C_{io}	Input-to-output internal capacitance	B port	3.3	1.65 to 3.3		5.5		pF

Electrical Characteristics (Cont.)

Timing Requirements: V_{CCA} = 1.5V ± 0.1 V

Over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1V (unless otherwise noted).

		V_{CCB} =1.8±0.15V		V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
DATA rate	Push-pull		40		60		60		60	Mbps
DATA rate	Open-drain		0.8		0.8		1		1	Mbps
t_W Pulse duration	Push-pull	25		16.7		16.7		16.7		ns
t_W Pulse duration	Push-pull	1250		1250		1000		1000		ns

Timing Requirements: V_{CCA} = 1.8V ± 0.15V

Over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (unless otherwise noted).

		V_{CCB} =1.8±0.15V		V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
DATA rate	Push-pull		45		65		70		70	Mbps
DATA rate	Open-drain		0.8		0.8		0.8		1	Mbps
t_W Pulse duration	Push-pull	22.2		15.3		15.3		15.3		ns
t_W Pulse duration	Push-pull	1250		1250		1250		1000		ns

Timing Requirements: V_{CCA} = = 2.5V ± 0.2V

Over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (unless otherwise noted).

		V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
DATA rate	Push-pull		80		95		100	Mbps
DATA rate	Open-drain		0.8		0.8		1	Mbps
t_W Pulse duration	Push-pull	12.5		10.5		10		ns
t_W Pulse duration	Push-pull	1250		1250		1000		ns

Electrical Characteristics (Cont.)

Timing Requirements: V_{CCA} = 3.3V ± 0.3V

Over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (unless otherwise noted).

		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	
DATA rate	Push-pull		100		110	Mbps
DATA rate	Open-drain		0.8		1.2	Mbps
t_W Pulse duration	Push-pull	10		9.1		ns
t_W Pulse duration	Push-pull	1250		833		ns

Switching Characteristics: V_{CCA} = 1.5V ± 0.1 V

Over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1 V (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CCB} =1.8±0.15V		V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL} Propagation delay time (high-to-low)	A-to-B Push-pull driving		11		9.2		8.6		8.6	ns
t_{PHL} Propagation delay time (high-to-low)	A-to-B Open-drain driving	4	14.4	3.6	12.8	3.5	12.2	3.5	12	ns
t_{PLH} Propagation delay time (low-to-high)	A-to-B Push-pull driving		12		10		9.8		9.7	ns
t_{PLH} Propagation delay time (low-to-high)	A-to-B Open-drain driving	182	720	143	554	114	473	81	384	ns
t_{PHL} Propagation delay time (high-to-low)	B-to-A Push-pull driving		12.7		11.1		11		12	ns
t_{PHL} Propagation delay time (high-to-low)	B-to-A Open-drain driving	3.4	13.2	3.1	9.6	2.8	8.5	2.5	7.5	ns
t_{PLH} Propagation delay time (low-to-high)	B-to-A Push-pull driving		9.5		6.2		5.1		1.8	ns
t_{PLH} Propagation delay time (low-to-high)	B-to-A Open-drain driving	186	745	147	603	118	519	84	407	ns
t_{EN} Enable time	OE-to A or B Push-pull driving		200		200		200		200	ns

Electrical Characteristics (Cont.)

Switching Characteristics: V_{CCA} = 1.5V ± 0.1 V

Over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1 V (unless otherwise noted).

PARA METER	TEST CONDITIONS	V_{CCB} =1.8±0.15V		V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DIS} Disable time	OE-to A or B Push-pull driving		400		400		400		400	ns
t_{rA} Input rise time	A-port rise time Push-pull driving	3.5	13.1	3	9.8	3.1	9	3.2	8.3	ns
t_{rA} Input rise time	A-port rise time Open-drain driving	147	982	115	716	92	592	66	481	ns
t_{rB} Input rise time	B-port rise time Push-pull driving	2.9	11.4	1.9	7.4	0.9	4.7	0.7	2.6	ns
t_{rB} Input rise time	B-port rise time Open-drain driving	135	1020	91	756	58	653	20	370	ns
t_{rA} Input fall time	A-port fall time Push-pull driving	2.3	9.9	1.7	7.7	1.6	6.8	1.7	6	ns
t_{rA} Input fall time	A-port fall time Open-drain driving	2.4	10	2.1	7.9	1.7	7	1.5	6.2	ns
t_{rB} Input fall time	B-port fall time Push-pull driving	2	8.7	1.3	5.5	0.9	3.8	0.8	3.1	ns
t_{rB} Input fall time	B-port fall time Open-drain driving	1.2	11.5	1.3	8.6	1	9.6	0.5	7.7	ns
$t_{SK(O)}$ Skew (time) output	Channel-to channel skew Push-pull driving		1	1	1		1.1		1	ns
Maximum data rate	A or B Push-pull driving	40		60		60		60		Mbps
Maximum data rate	A or B Open-drain driving	0.8		0.8		1		1		Mbps

Electrical Characteristics (Cont.)

Switching Characteristics: V_{CCA} = 1.8V ± 0.15 V

Over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15 V (unless otherwise noted).

PARA METER	TEST CONDITIONS	V_{CCB} =1.8±0.15V		V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL} Propagation delay time (high-to-low)	A-to-B Push-pull driving		8.2		6.4		5.7		5.6	ns
t_{PHL} Propagation delay time (high-to-low)	A-to-B Open-drain driving	3.6	11.4	3.2	9.9	3.1	9.3	3.1	8.9	ns
t_{PLH} Propagation delay time (low-to-high)	A-to-B Push-pull driving		9		8.2		6.5		6.3	ns
t_{PLH} Propagation delay time (low-to-high)	A-to-B Open-drain driving	194	729	155	584	126	466	90	346	ns
t_{PHL} Propagation delay time (high-to-low)	B-to-A Push-pull driving		9.8		8		7.4		7	ns
t_{PHL} Propagation delay time (high-to-low)	B-to-A Open-drain driving	3.4	12.1	2.8	8.5	2.5	7.3	2.1	6.2	ns
t_{PLH} Propagation delay time (low-to-high)	B-to-A Push-pull driving		10.2		7		5.8		5	ns
t_{PLH} Propagation delay time (low-to-high)	B-to-A Open-drain driving	197	733	159	578	129	459	93	323	ns
t_{EN} Enable time	OE-to A or B Push-pull driving		200		200		200		200	ns
t_{DIS} Disable time	OE-to A or B Push-pull driving		410		410		410		410	ns
t_{rA} Input rise time	A-port rise time Push-pull driving	3.1	11.9	2.6	8.6	2.7	7.8	2.8	7.2	ns
t_{rA} Input rise time	A-port rise time Open-drain driving	155	996	124	691	100	508	72	350	ns
t_{rB} Input rise time	B-port rise time Push-pull driving	2.8	10.5	1.8	7.2	1.2	5.2	0.7	2.7	ns
t_{rB} Input rise time	B-port rise time Open-drain driving	132	1001	106	677	73	546	32	323	ns

Electrical Characteristics (Cont.)

Switching Characteristics: V_{CCA} = 1.8V ± 0.15 V

Over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15 V (unless otherwise noted).

PARA METER	TEST CONDITIONS	V_{CCB} =1.8±0.15V		V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{rA} Input fall time	A-port fall time Push-pull driving	2.1	8.8	1.6	6.6	1.4	5.7	1.4	4.9	ns
t_{rA} Input fall time	A-port fall time Open-drain driving	2.2	9	1.7	6.7	1.4	5.8	1.2	5.2	ns
t_{rB} Input fall time	B-port fall time Push-pull driving	2	8.3	1.3	5.4	0.9	3.9	0.7	3	ns
t_{rB} Input fall time	B-port fall time Open-drain driving	0.8	10.5	0.7	10.7	1	9.6	0.6	7.6	ns
$t_{SK(O)}$ Skew (time) output	Channel-to channel skew Push-pull driving		1		1		1		1	ns
Maximum data rate	A or B Push-pull driving	40		60		60		60		Mbps
Maximum data rate	A or B Open-drain driving	0.8		0.8		0.8		1		Mbps

Switching Characteristics: V_{CCA} = 2.5V ± 0.2 V

Over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2 V (unless otherwise noted).

PARA METER	TEST CONDITIONS	V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL} Propagation delay time (high-to-low)	A-to-B Push-pull driving		5		4		3.7	ns
t_{PHL} Propagation delay time (high-to-low)	A-to-B Open-drain driving	2.4	6.9	2.3	6.3	2.2	5.8	ns
t_{PLH} Propagation delay time (low-to-high)	A-to-B Push-pull driving		5.2		4.3		3.9	ns
t_{PLH} Propagation delay time (low-to-high)	A-to-B Open-drain driving	149	592	125	488	93	368	ns

Electrical Characteristics (Cont.)

Switching Characteristics: V_{CCA} = 2.5V ± 0.2 V

Over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2 V (unless otherwise noted).

PARA METER	TEST CONDITIONS	V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL} Propagation delay time (high-to-low)	B-to-A Push-pull driving		5.4		4.7		4.2	ns
t_{PHL} Propagation delay time (high-to-low)	B-to-A Open-drain driving	2.5	7.3	2.2	6	1.8	4.9	ns
t_{PLH} Propagation delay time (low-to-high)	B-to-A Push-pull driving		5.9		4.4		3.5	ns
t_{PLH} Propagation delay time (low-to-high)	B-to-A Open-drain driving	150	595	126	481	94	345	ns
t_{EN} Enable time	OE-to A or B Push-pull driving		200		200		200	ns
t_{DIS} Disable time	OE-to A or B Push-pull driving		400		400		400	ns
t_{rA} Input rise time	A-port rise time Push-pull driving	2	7.3	2.1	6.4	2.2	5.8	ns
t_{rA} Input rise time	A-port rise time Open-drain driving	110	692	93	529	68	369	ns
t_{rB} Input rise time	B-port rise time Push-pull driving	1.8	6.5	1.3	5.1	0.7	3.4	ns
t_{rB} Input rise time	B-port rise time Open-drain driving	107	693	79	483	41	304	ns
t_{rA} Input fall time	A-port fall time Push-pull driving	1.5	5.7	1.2	4.7	1.3	3.8	ns
t_{rA} Input fall time	A-port fall time Open-drain driving	1.5	5.6	1.2	4.7	1.1	4	ns
t_{rB} Input fall time	B-port fall time Push-pull driving	1.4	5.4	0.9	4.1	0.7	3	ns
t_{rB} Input fall time	B-port fall time Open-drain driving	0.4	14.2	0.5	19.4	0.4	3	ns

Electrical Characteristics (Cont.)

Switching Characteristics: V_{CCA} = 2.5V ± 0.2 V

Over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2 V (unless otherwise noted).

PARA METER	TEST CONDITIONS	V_{CCB} = 2.5±0.2V		V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SK(0)}$ Skew (time) output	Channel-to channel skew Push-pull driving		1		1.2		1	ns
Maximum data rate	A or B Push-pull driving	60		60		60		Mbps
Maximum data rate	A or B Open-drain driving	0.8		0.8		1		Mbps

Switching Characteristics: V_{CCA} = 3.3V ± 0.3 V

Over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3 V (unless otherwise noted).

PARA METER	TEST CONDITIONS	V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	
t_{PHL} Propagation delay time (high-to-low)	A-to-B Push-pull driving		3.8		3.1	ns
t_{PHL} Propagation delay time (high-to-low)	A-to-B Open-drain driving	2	5.3	1.9	4.8	ns
t_{PLH} Propagation delay time (low-to-high)	A-to-B Push-pull driving		3.9		3.5	ns
t_{PLH} Propagation delay time (low-to-high)	A-to-B Open-drain driving	111	439	87	352	ns
t_{PHL} Propagation delay time (high-to-low)	B-to-A Push-pull driving		4.2		3.8	ns
t_{PHL} Propagation delay time (high-to-low)	B-to-A Open-drain driving	2.1	5.5	1.7	4.5	ns
t_{PLH} Propagation delay time (low-to-high)	B-to-A Push-pull driving		3.8		4.3	ns
t_{PLH} Propagation delay time (low-to-high)	B-to-A Open-drain driving	112	449	86	339	ns

Electrical Characteristics (Cont.)

Switching Characteristics: V_{CCA} = 3.3V ± 0.3 V

Over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3 V (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CCB} = 3.3±0.3V		V_{CCB} = 5±0.5V		Unit
		Min.	Max.	Min.	Max.	
t_{EN} Enable time	OE-to A or B Push-pull driving		200		200	ns
t_{DIS} Disable time	OE-to A or B Push-pull driving		400		400	ns
t_{rA} Input rise time	A-port rise time Push-pull driving	1.8	5.7	1.9	5	ns
t_{rA} Input rise time	A-port rise time Open-drain driving	75	446	57	337	ns
t_{rB} Input rise time	B-port rise time Push-pull driving	1.5	5	1	3.6	ns
t_{rB} Input rise time	B-port rise time Open-drain driving	72	427	40	290	ns
t_{rA} Input fall time	A-port fall time Push-pull driving	1.2	4.5	1.1	3.5	ns
t_{rA} Input fall time	A-port fall time Open-drain driving	1.1	4.4	1	3.7	ns
t_{rB} Input fall time	B-port fall time Push-pull driving	1.1	4.2	0.8	3.1	ns
t_{rB} Input fall time	B-port fall time Open-drain driving	1.1	4.2	0.8	3.1	ns
$t_{SK(0)}$ Skew (time) output	Channel-to channel skew Push-pull driving		1		1	ns
Maximum data rate	A or B Push-pull driving	60		60		Mbps
Maximum data rate	A or B Open-drain driving	0.8		1.2		Mbps

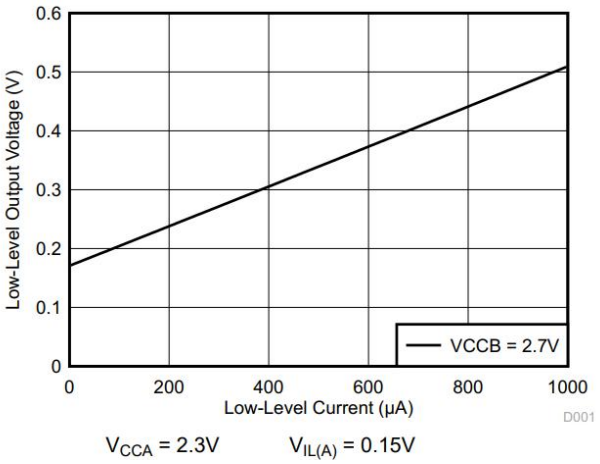
Electrical Characteristics (Cont.)

Operating Characteristics: V_{CCA} = 1.5 to 3.3V,V_{CCB} = 1.5 to 3.3V

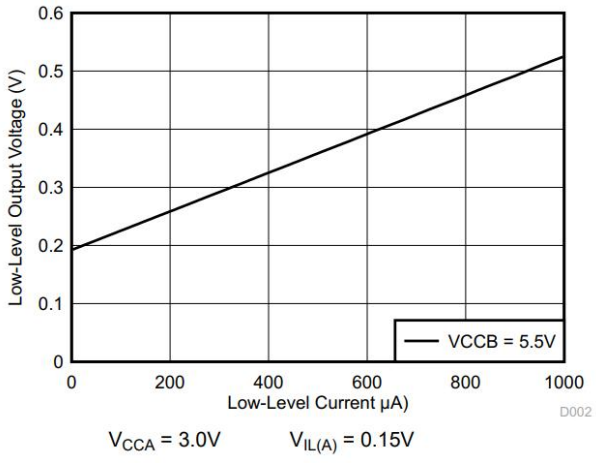
T_A = 25°C,C_L=0pf ,f = 10MHz,tr= tf= 1ns,OE =V_{CCA},(outputs enabled).

PARA METER	TEST CONDITIONS	V_{CCA}=V_{CCB} =1.5V		V_{CCA}=V_{CCB} =1.8V		V_{CCA}=V_{CCB} =2.5V		V_{CCA}=V_{CCB} =3.3V		Unit
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
C_{pdA} Power dissipation capacitance	A-port input B-port output	5.9		5.9		6.7		8		pF
C_{pdA} Power dissipation capacitance	B-port input A-port output	9.9		9.7		9.7		9.8		pF
C_{pdB} Power dissipation capacitance	A-port input B-port output	21.6		20.8		21		23		pF
C_{pdB} Power dissipation capacitance	B-port input A-port output	16.7		16.8		17.8		20.90		pF
C_{pdA} Power dissipation capacitance	A-port input B-port output	0.01		0.01		0.01		0.01		pF
C_{pdA} Power dissipation capacitance	B-port input A-port output	0.01		0.01		0.01		0.01		pF
C_{pdB} Power dissipation capacitance	A-port input B-port output	0.01		0.01		0.01		0.02		pF
C_{pdB} Power dissipation capacitance	B-port input A-port output	0.01		0.01		0.01		0.02		pF

Typical Characteristics



Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

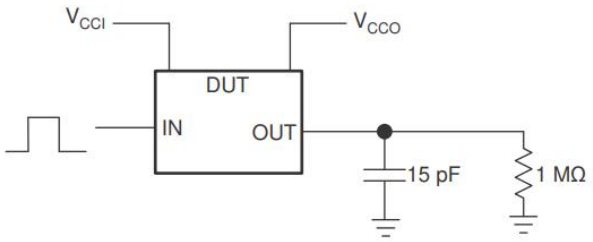


Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

Parameter Measurement Information

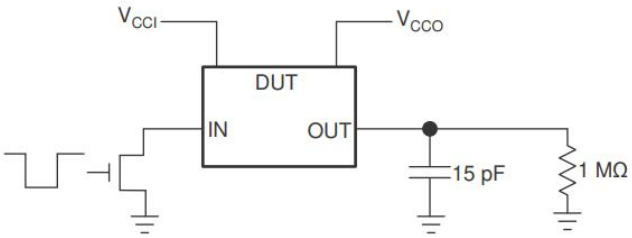
Load Circuits

Figure shows the push-pull driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time. Figure 2 shows the open-drain driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time.



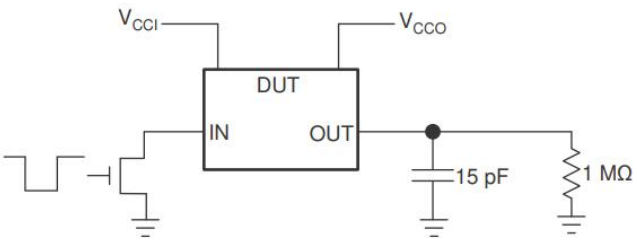
A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.

Figure 1. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver



A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.

Figure 2. Data Rate (15pF), Pulse Duration (15pF), Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.

Figure 3. Load Circuit for Enable-Time and Disable-Time Measurement

Parameter Measurement Information (Cont.)

Voltage Waveforms

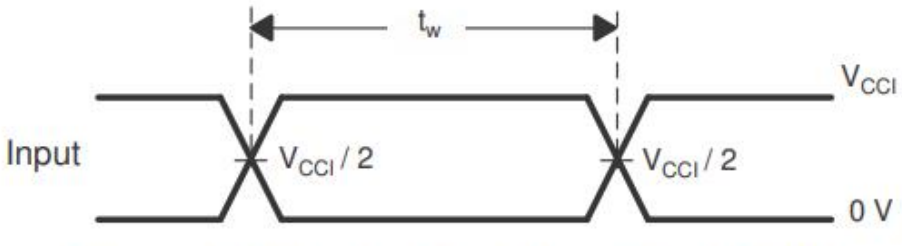


Figure 4. Pulse Duration (Push-Pull)

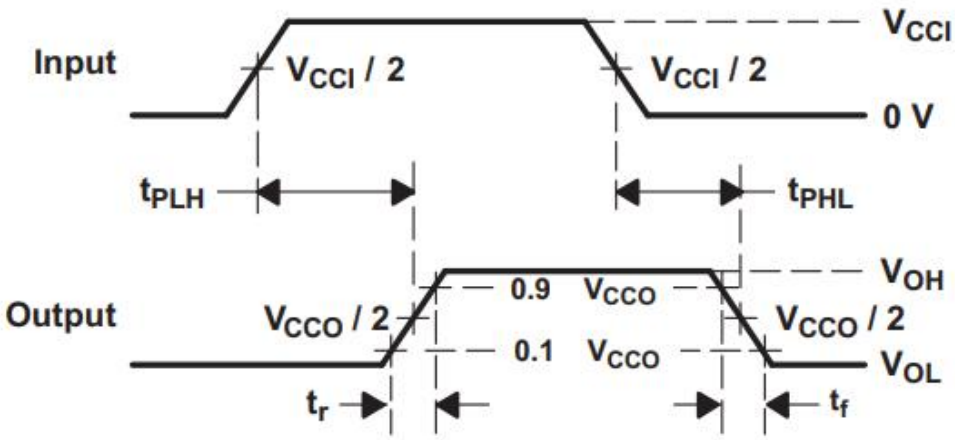


Figure 5. Propagation Delay Times

Detailed Description

Overview

The LTLB0104 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.4V to 3.6V. The B-port accepts I/O voltages from 1.65V to 5.5V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

Functional Block Diagram

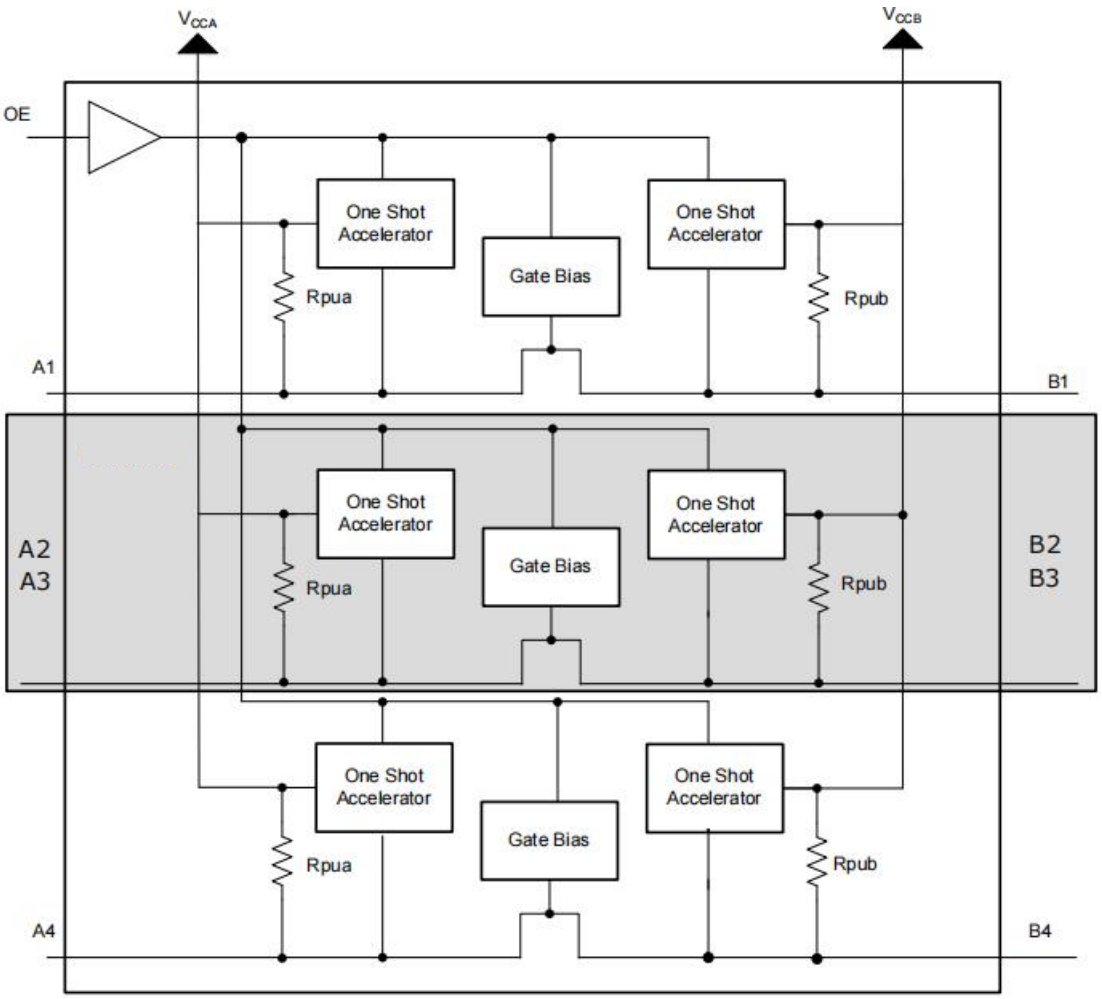


Figure 6. Functional Block Diagram

Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving high. R_{PUA} 10 and R_{PUB} are disabled when OE = Low.

Feature Description

Architecture

Figure shows semi-buffered architecture design this application requires for both push-pull and open-drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of 300Ω to 500Ω) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design does not need a direction control signal to control the direction of data flow from A to B or from B to A. The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

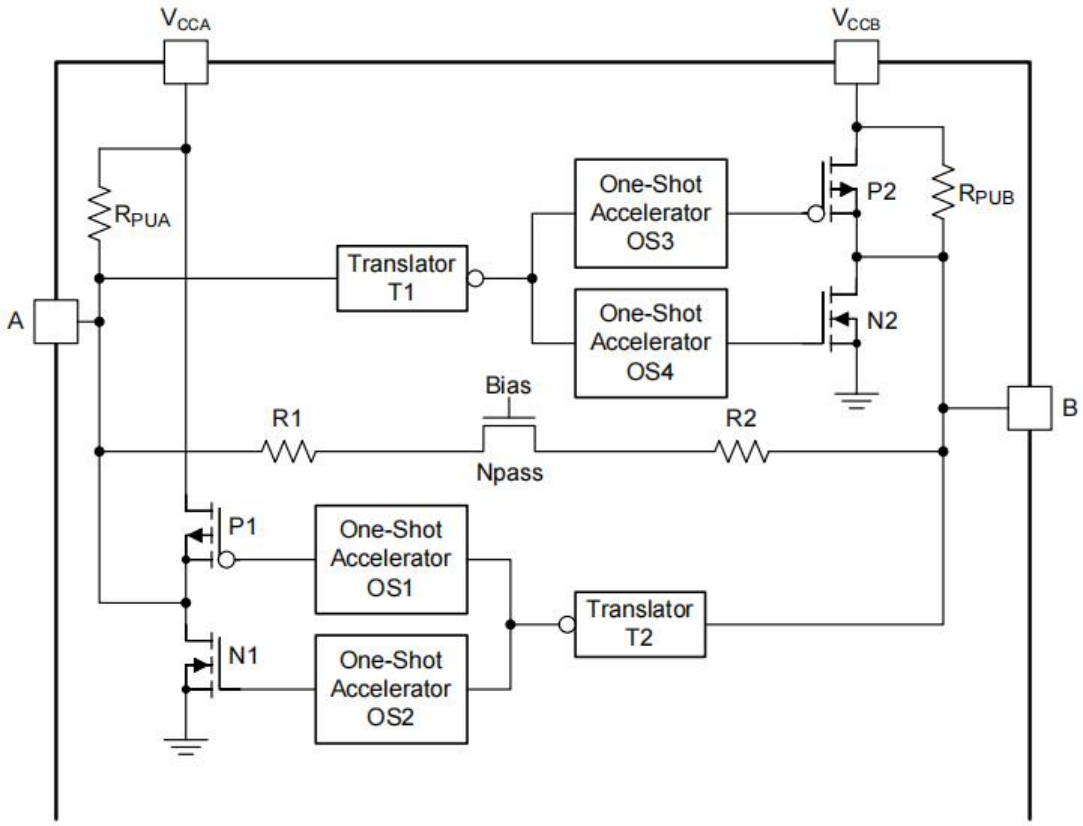


Figure 7. Architecture of a LTLB0104 cell

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4. Transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and this speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

Feature Description (Cont.)

Input Driver Requirement

The continuous DC-current sinking capability is determined by the external system-level open-drain (or pushpull) drivers that are interfaced to the LTLB0104 I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current sourcing capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.
The fall time (tfA, tfB) of a signal depends on the edge-rate and output impedance of the external device driving LTLB0104 data I/Os, as well as the capacitive loading on the data lines.
Similarly, the tPHL and maximum data rates also depend on the output impedance of the external driver. The values for tfA, tfB, tPHL, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

Output Load Considerations

Linearin recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and so that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by allowing any reflection to see a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 30ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the LTLB0104 output. Therefore, Linearin recommends careful PCB layout practices that this lumped load capacitance is considered to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

Enable and Disable

The LTLB0104 has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time (tDIS) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time (tEN) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

Pull-up or Pull-down Resistors on I/O Lines

The LTLB0104 has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to VCCA and each B-port I/O has a pull-up resistor (R_{PUB}) to VCCB. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower VOL values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

Device Functional Modes

The LTLB0104 device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

Application and Implementation

Application Information

The LTLB0104 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is an excellent choice for use in applications where an open-drain driver is connected to the data I/Os. The device is appropriate for applications where a push-pull driver is connected to the data I/Os. The device is a semi-buffered auto-direction-sensing voltage translator design is optimized for translation applications (for example, MMC Card Interfaces) that require the system to start out in a low-speed open-drain mode and then switch to a higher speed push-pull mode.

Typical Application

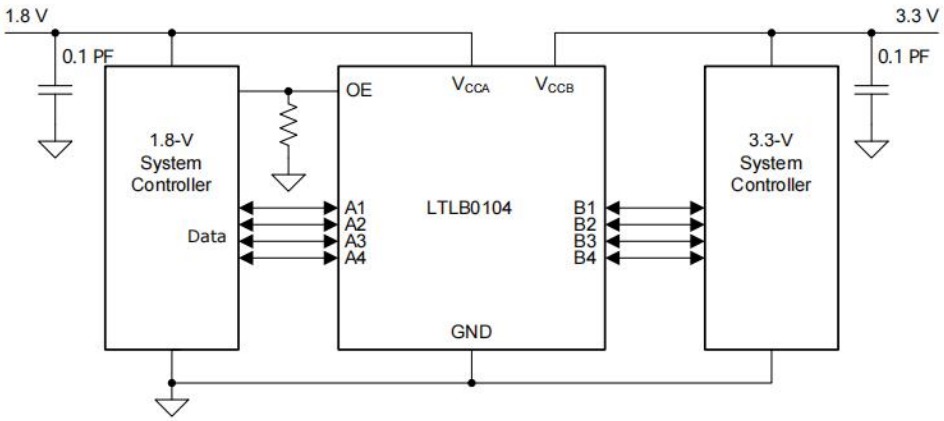


Figure 8. Typical Application Circuit

Design Requirements

For this design example, use the parameters listed in Table 1.Ensure that $V_{CCA} < V_{CCB}$.

Table 1. Design Parameters

Design Parameter	Example Value
Input voltage range	1.4V to 3.6V
Output voltage range	1.65V to 5.5V

Detailed Design Procedure

To begin the design process, determine the following:
Input voltage range
– Use the supply voltage of the device that is driving the LTLB0104 device to determine the input voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.
Output voltage range
– Use the supply voltage of the device that the LTLB0104 device is driving to determine the output voltage range.

Application and Implementation (Cont.)

Detailed Design Procedure (Cont.)

– The LTLB0104 device has smart internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary.
An external pull-down resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 to calculate the V_{OH} as a result of an external pull-down resistor.
1. $V_{OH} = V_{CC}x \times R_{PD} / (R_{PD} + 4k\Omega)$

Application Curves

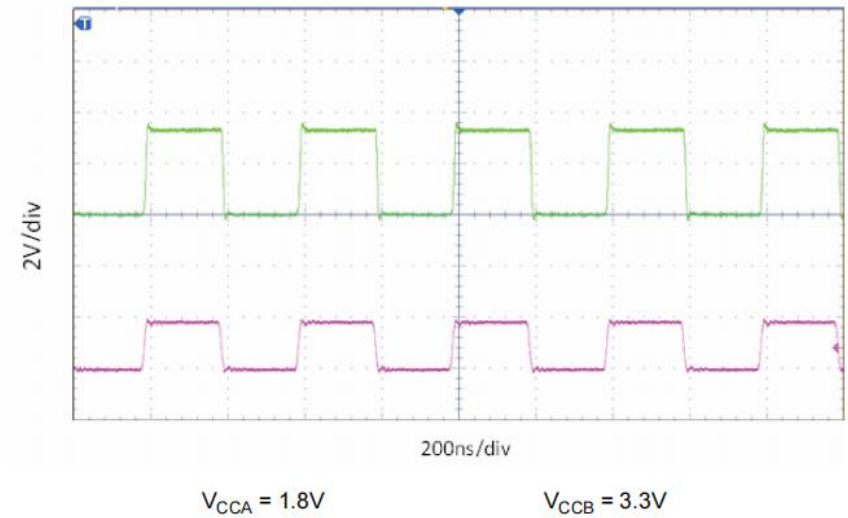


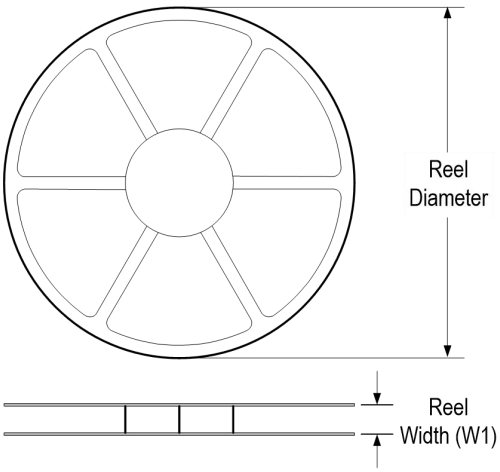
Figure 9. Level-Translation of a 2.5MHz Signal

Power Supply Recommendations

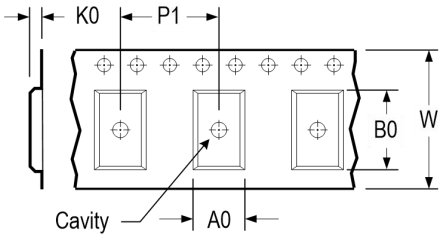
During operation, ensure that V_{CCA}, V_{CCB} at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To put the outputs in the high-impedance state during power up or power down, tie the OE input pin to GND through a pull-down resistor, and do not enable the OE input until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pull-down resistor to ground.

Tape and Reel Information

REEL DIMENSIONS

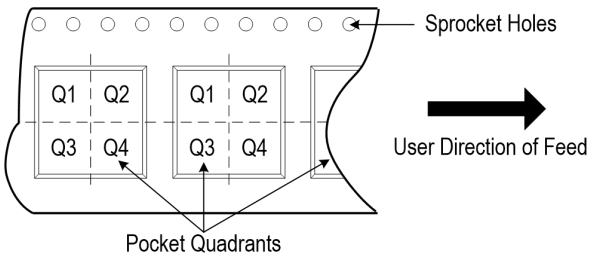


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

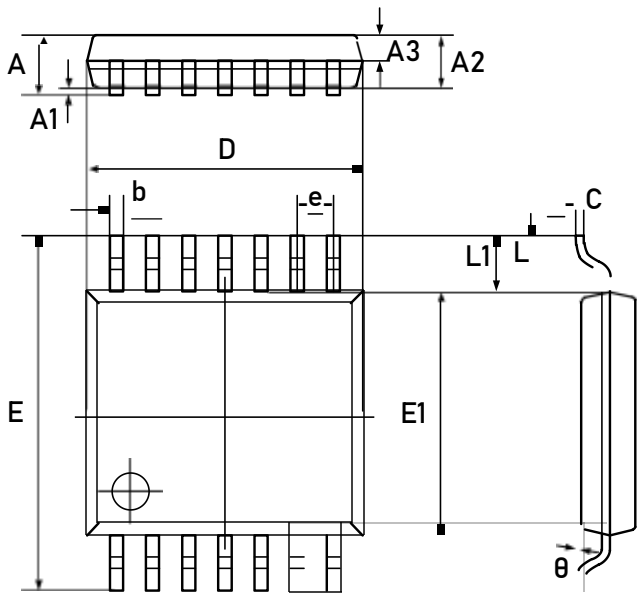


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTLB0104YT14/R6	TSSOP	14	3 000	330	16.5	6.9	5.5	1.3	8.0	16.0	Q1

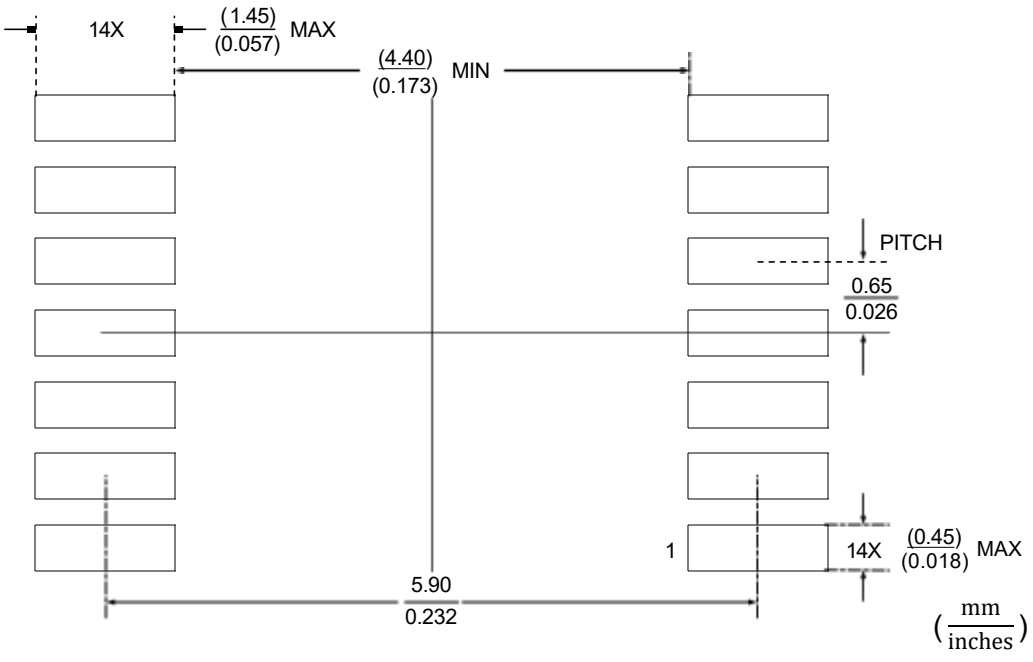
Package Dimension

DIMENSIONS, TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
A3	0.390	0.490	0.015	0.019
b	0.200	0.290	0.008	0.011
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.191	0.199
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 TYP.		0.026 TYP.	
L1	1.000 REF.		0.039 REF.	
L	0.450	0.750	0.018	0.030
θ	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L



Important Notice

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