LTLP9306

Dual Bidirectional I²C Bus and SMBus Voltage-Level Translator

General Description

The LTLP9306 device is a dual bidirectional I²C and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.2V to 3.3V V_{REF1} and 1.8V to 5.5V V_{REF2}.

The LTLP9306 device allows bidirectional voltage translations between 1.2V and 5V, without the use of a direction pin. The low ON-state resistance (RON) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In addition to voltage translation, the LTLP9306 device can be used to isolate a 400kHz bus from a 100kHz bus by controlling the EN pin to disconnect the slower bus during fast mode communication.

Features and Benefits

- 2-Bit bidirectional translator for SDA and SCL lines in mixed-mode I²C Applications
- I²C and SMBus compatible
- Less than 1.5-ns maximum propagation delay to accommodate standard-mode and fast-mode I²C devices and multiple controllers
- Allows voltage-level translation between
  - 1.0V V_{REF1} and 1.2V, 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
  - 1.2V V_{REF1} and 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
  - 1.8V V_{REF1} and 2.5V, 3.3V, or 5V V_{REF2}
  - 2.5V V_{REF1} and 3.3V or 5V V_{REF2}
  - 3.3V V_{REF1} and 5V V_{REF2}
- Provides bidirectional voltage translation with no direction pin
- Low 3.5Ω ON-state resistance between input and output ports provides less signal distortion
- Open-drain I²C I/O ports (SCL1, SDA1, SCL2, and SDA2)
- 5V Tolerant I²C I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2, and SDA2 pins for EN = low
- Lockup-free operation for isolation when EN = low
- Flow-through pinout for ease of printed-circuitboard trace routing
- Latch-up performance exceeds 100 mA Per JESD 78, class II

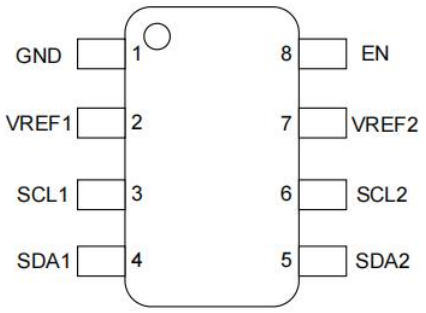
Applications

- I²C, SMBus, PMBus, MDIO, UART, low-speed DIO,GPIO and other two-signal interfaces
- Servers
- Routers (telecom switching equipment)
- Personal Computers
- Industrial Automation

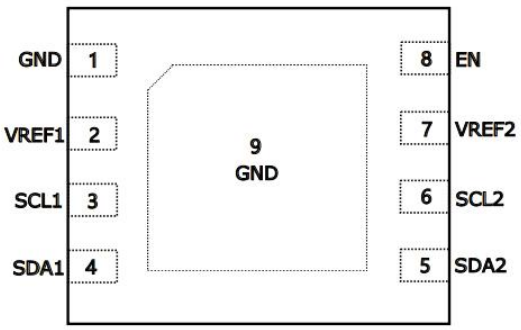
LINEARIN

Pin Description (Top View)

LTLP9306
MSOP-8L



LTLP9306
DFN2x3-8L



Pin Function

Symbol	PackageNC		Function
	MSOP-8L	DFN2x3-8L	
GND	1	1/9	Ground, 0V
VREF1	2	2	Low-voltage-side reference supply voltage for SCL1 and SDA1
SCL1	3	3	Serial clock, low-voltage side
SDA1	4	4	Serial data, low-voltage side
SDA2	5	5	Serial data, high-voltage side
SCL2	6	6	Serial clock, high-voltage side
VREF2	7	7	High-voltage-side reference supply voltage for SCL2 and SDA2
EN	8	8	Power pin

Ordering Information

Package Type	Part Number	Quantity	Mark Code
MSOP-8L	LTLP9306YV8/R6	Tape and Reel, 3 000	9306
DFN2x3-8L	LTLP9306YF8/R6	Tape and Reel, 3 000	9306

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC reference voltage range	V_{REF1}	-0.5	7	V
DC reference bias voltage range	V_{REF2}	-0.5	7	V
Input voltage range	V_I	-0.5	7	V
Input/output voltage range	$V_{I/O}$	-0.5	7	V
Continuous channel current			128	mA
Input clamp current (V_I<0)	I_{IK}		-150	mA
Maximum junction temperature	$T_{j(max)}$		125	℃
Storage Temperature Range	T_{stg}	-65	150	℃

ESD Ratings

Parameter	Level	Unit
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2 000	V
Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	±500	

Recommended Operating Conditions

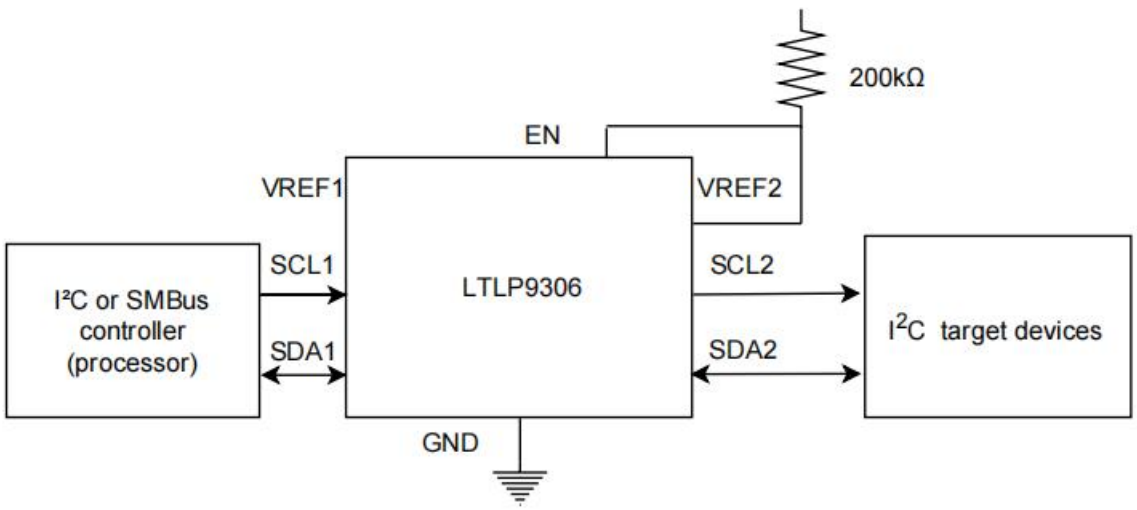
Symbol	Parameter	Min	Max	Unit
V_{REF1}	Reference voltage	0	5.5	V
V_{REF2}	Reference voltage	0	5.5	V
$V_{I/O}$	Input/output voltage（SCL1,SDA1, SCL2, SDA2）	0	5.5	V
EN	Enable input voltage	0	5.5	V
I_{PASS}	Pass switch current		64	mA
T_A	Operating ambient temperature	-40	+85	℃

Electrical Characteristics

Over recommended operating ambient temperature range (unless otherwise noted).

Parameter	Symbol	Test Conditions			Min	Typ	Max	Unit
Input clamp voltage	V_{IK}	I_I=-18mA, EN=0V					-1.2	V
Input leakage current	I_{IH}	V_I=5V, EN=0V					5	µA
Input capacitance	$C_{i(EN)}$	V_I=3V or 0				11		pF
Off capacitance	$C_{io(off)}$	SCLn,SDAn, V_O=3V or 0, EN=0V				4	6	pF
On capacitance	$C_{io(on)}$	SCLn,SDAn, V_O=3V or 0, EN=3V				10.5	12.5	pF
On-state resistance	R_{ON}	SCLn,SDAn	V_I=0	I_O=64mA, EN=4.5V		3.5	5.5	Ω
				I_O=64mA, EN=3V		4.7	7	
				I_O=64mA, EN=2.3V		6.3	9.5	
			V_I=0	I_O=15mA, EN=1.5V		25.5	32	
			V_I=2.4V	I_O=15mA, EN=4.5V	1	6	15	
				I_O=15mA, EN=3V	20	60	140	
			V_I=1.7V	I_O=15mA,EN=2.3V	20	60	140	

Typical Application Circuit



Switching Characteristics AC Performance (Translating Down)

Over recommended operating ambient temperature range, EN = 3.3V, V_{IH} = 3.3V, V_{IL} = 0, V_M = 1.15V (unless otherwise noted)

Parameter	From (INPUT)	To (OUTPUT)	CL=50pF		CL=30pF		CL=15pF		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

Over recommended operating ambient temperature range, EN = 2.5V, V_{IH}= 3.3V, V_{IL} = 0, V_M = 0.75V (unless otherwise noted)

Parameter	From (INPUT)	To (OUTPUT)	CL=50pF		CL=30pF		CL=15pF		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
t_{PHL}			0	1.3	0	1	0	0.6	

Over recommended operating ambient temperature range, EN = 3.3V, V_{IH} = 2.3V, V_{IL} = 0, V_T = 3.3V, V_M = 1.15V, R_L = 300Ω (unless otherwise noted)

Parameter	From (INPUT)	To (OUTPUT)	CL=50pF		CL=30pF		CL=15pF		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

Over recommended operating ambient temperature range, EN = 2.5V, V_{IH} = 2.3V, V_{IL} = 0, V_T = 3.3V, V_M = 0.75V, R_L = 300Ω (unless otherwise noted)

Parameter	From (INPUT)	To (OUTPUT)	CL=50pF		CL=30pF		CL=15pF		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	1	0	0.6	0	0.4	ns
t_{PHL}			0	1.3	0	1.3	0	0.8	

Parameter Measurement Information

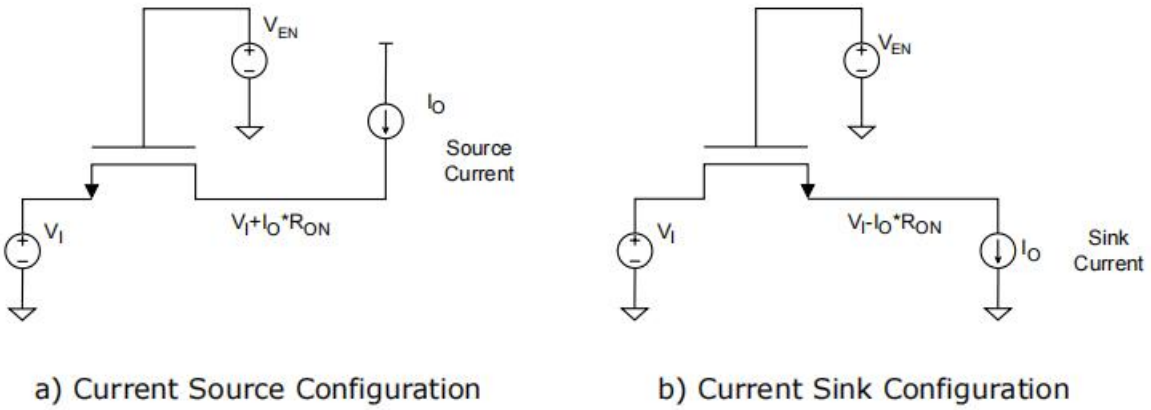
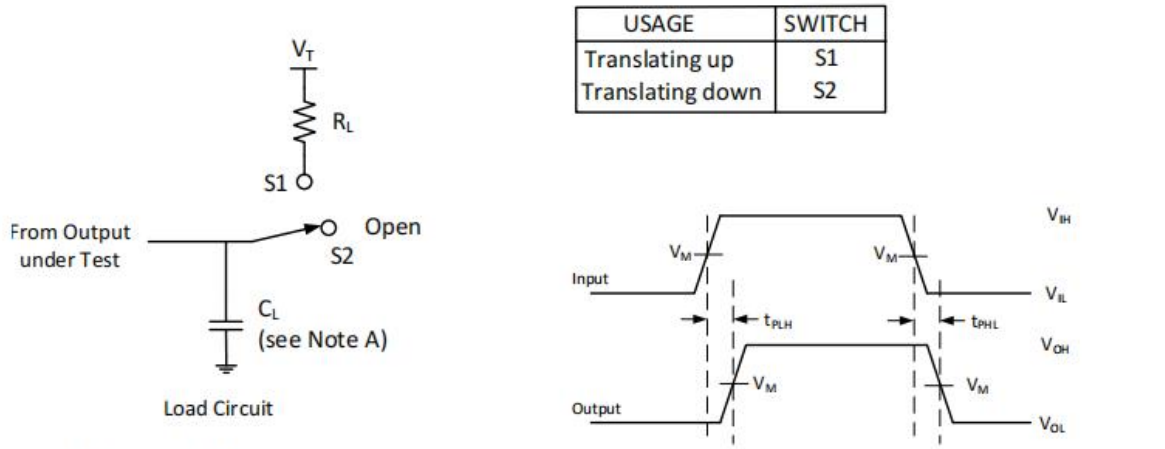


Figure 1:Current Source and Current Sink Configurations for RON Measurements



USAGE	SWITCH
Translating up	S1
Translating down	S2

NOTES: A. C_L includes probe and jig capacitance
B. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50 Ω, t_r≤2 ns, t_f ≤2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 2:Load Circuit for Outputs

Detailed Description

Overview

The LTLP9306 device is a dual bidirectional I²C and SMBus voltage-level translator with an enable (EN) input and operates without use of a direction pin. The voltage supply range for V_{REF1} is 1.2V to 3.3V and the supply range for V_{REF2} is 1.8V to 5.5V.

The LTLP9306 device can also be used to run two buses, one at 400kHz operating frequency and the other at 100kHz operating frequency. If the two buses are operating at different frequencies, the 100kHz bus must be disconnected by using the EN pin when the 400kHz operation of the main bus is required. If the controller is running at 400kHz, the maximum system operating frequency may be less than 400kHz because of the delays added by the level shifter.

In I²C applications, the bus capacitance limit of 400pF restricts the number of devices and bus length. The capacitive load on both sides of the LTLP9306 device must be taken into account when approximating the total load of the system, ensuring the sum of both sides is under 400pF.

Both the SDA and SCL channels of the LTLP9306 device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage-translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less-ESD-resistant devices.

Definition of threshold voltage

This document references a threshold voltage denoted as V_{th}, which appears multiple times throughout this document when discussing the NFET between V_{REF1} and V_{REF2}. The value of Vth is approximately 0.6V at room temperature.

Correct Device Set Up

In a normal set up shown in the figure 3, the enable pin and V_{REF2} are shorted together and tied to a 200kΩ resistor and a reference voltage equal to V_{REF1} plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.

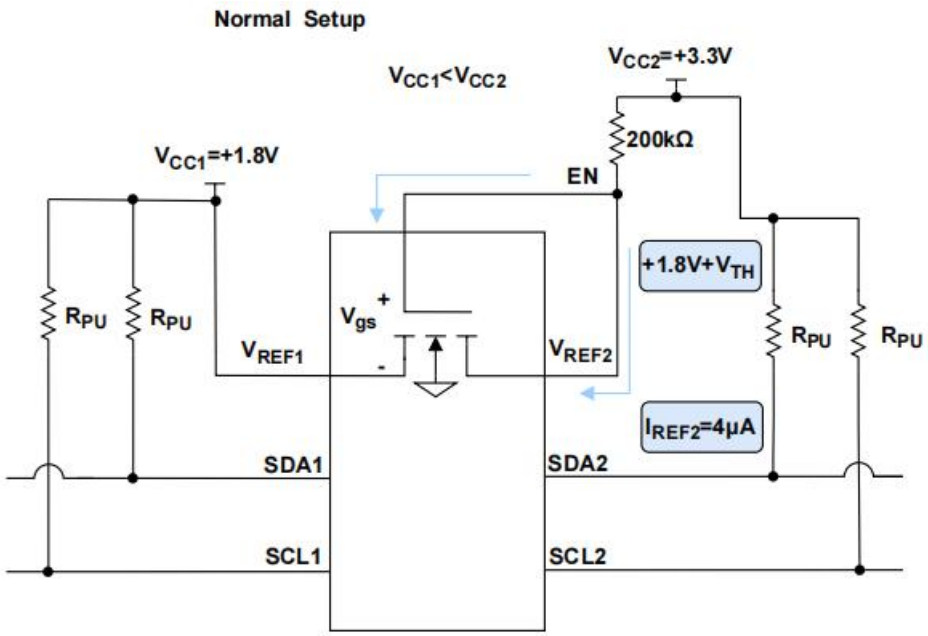


Figure 3:Normal Setup

Detailed Description (Cont.)

Care should be taken to ensure V_{REF2} has an external resistor tied between it and V_{CC2}. If V_{REF2} is tied directly to the V_{CC2} rail without a resistor, then there is no external resistance from the V_{CC2} to V_{CC1} to limit the current such as in figure 4. This effectively looks like a low impedance path for current to travel through and potentially break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in section 5.1. The continuous channel current is larger with a higher voltage difference between V_{CC1} and V_{CC2}.

The figure 4 shows an improper set up. If V_{CC2} is larger than V_{CC1} but less than V_{th}, the impedance between V_{CC1} and V_{CC2} is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when V_{CC2} becomes larger than V_{CC1} by V_{th}. During this event, the NFET turns on and begins to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.

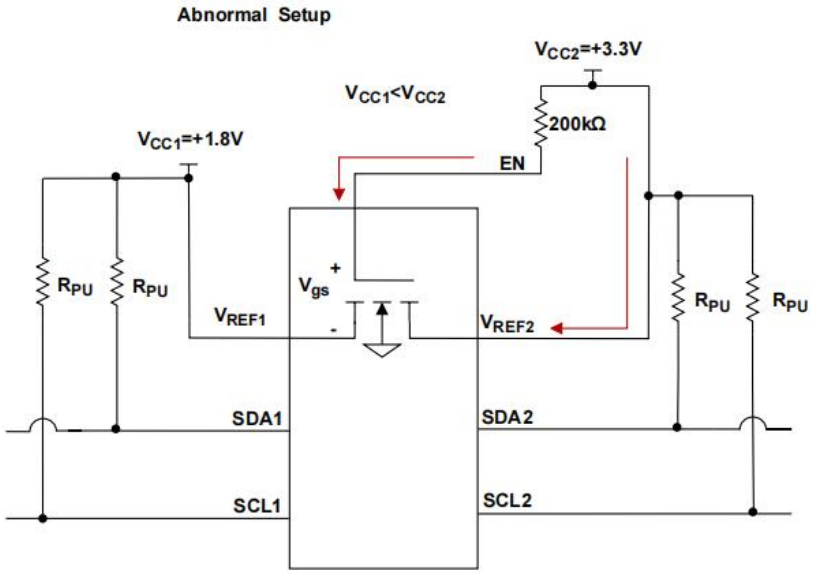


Figure 4:Abnormal Setup

Disconnecting an I²C target from the Main I²C Bus Using the EN Pin

LTLP9306 can be used as a switch to disconnect one side of the device from the main I²C bus. This can be advantageous in multiple situations. One instance of this situation is if there are devices on the I²C bus which only supports fast mode (400kHz) while other devices on the bus support fast mode plus (1MHz). An example of this is displayed in the figure 5.

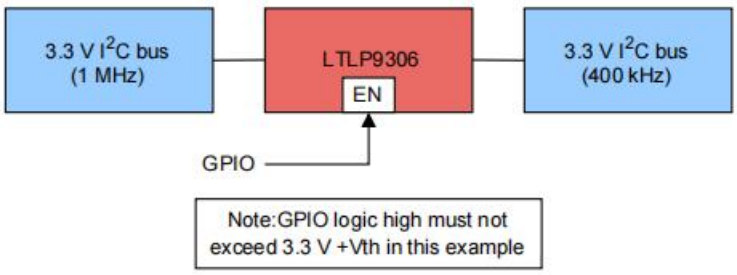


Figure 5:Example of an I²C bus with multiple supported frequencies

In this situation, if the controller is on the 1MHz side then communicating at 1MHz should not be attempted if LTLP9306 were enabled. It needs to be disabled for LTLP9306 to avoid possibly glitching state machines in devices which were designed to operate correctly at 400kHz or slower. When LTLP9306 is disabled, the controller can communicate with the 1MHz devices without disturbing the 400kHz bus. When the LTLP9306 is enabled, communication across both sides at 400kHz is acceptable.

Detailed Description (Cont.)

Supporting Remote Board Insertion to Backplane with LTLP9306

Another situation where LTLP9306 is advantageous when is using its enable feature is when a remote board with I²C lines needs to be attached to a main board (backplane) with an I²C bus such as in figure6. If connecting a remote board to a backplane is not done properly, the connection could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line, which could glitch an I²C device state machine causing the I²C bus to get stuck.

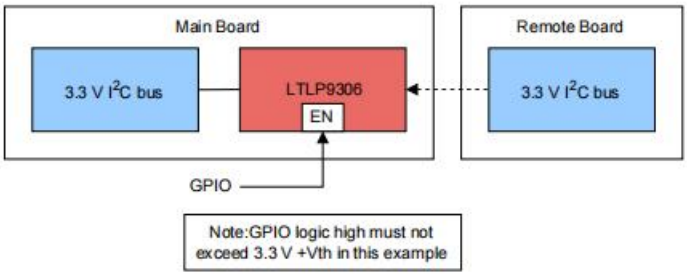


Figure 6:An example of connecting a remote board to a main board (backplane)

LTLP9306 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

Switch Configuration

LTLP9306 has the capability of being used with its V_{REF1} voltage equal to V_{REF2}. This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in figure 7 and translation mode is shown in figure 8.

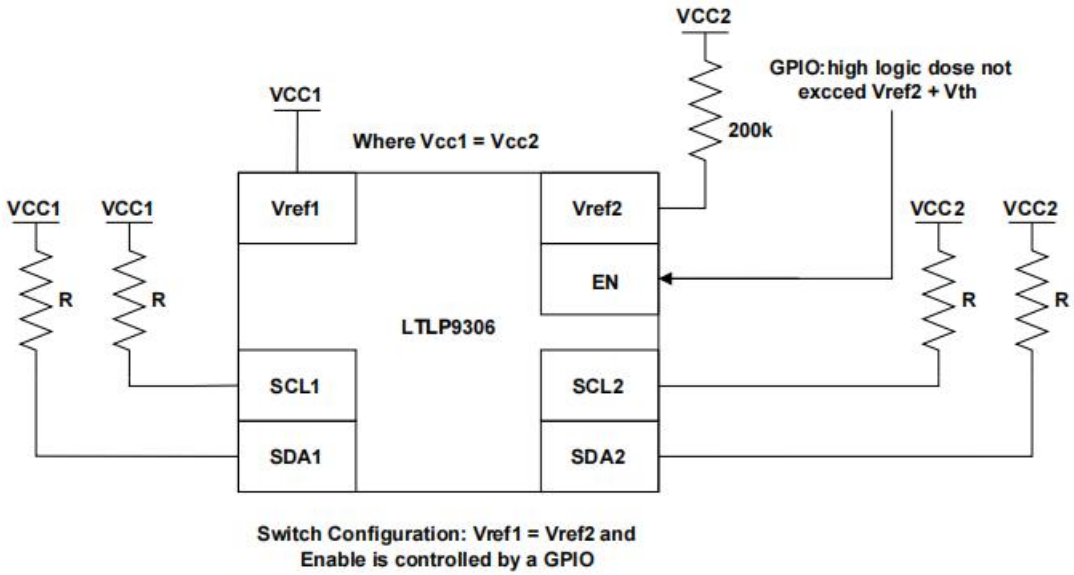


Figure 7:Switch Configuration

Detailed Description (Cont.)

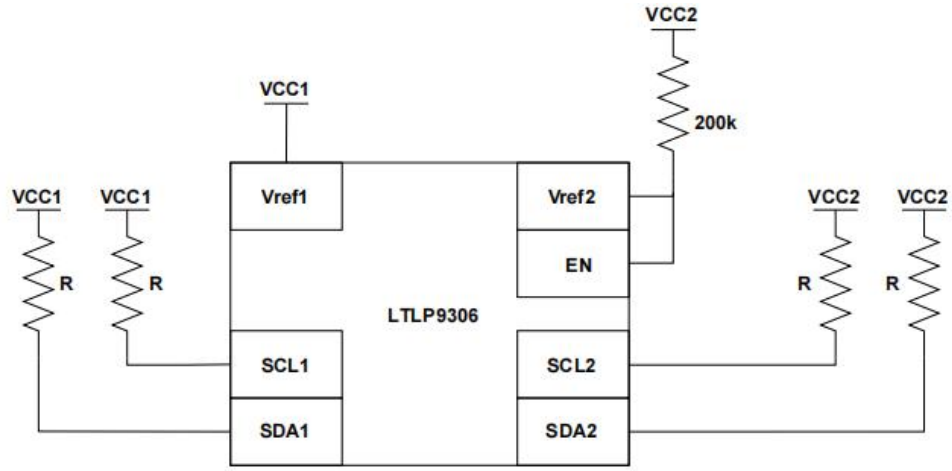


Figure 8:Translation Configuration

When LTLP9306 is in the switch configuration (V_{REF1} = V_{REF2}), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the LTLP9306 has the same propagation delay from side one to two and side two to one. The propagation delays become lower when V_{CC1}/V_{CC2} is larger. For example, the propagation delay at 1.8V is longer than at 5V in the switching configuration. When LTLP9306 is in translation mode, side one propagate lows to side two faster than side two can propagate lows to side 1. This time difference becomes larger the larger the difference between V_{CC2} and V_{CC1} becomes.

Controller on Side 1 or Side 2 of Device

I²C and SMBus are bidirectional protocols meaning devices on the bus can both transmit and receive data. LTLP9306 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the controller to be able to be placed on either side of the device. The figure 9 shows the controller on side two as opposed to the diagram on page 1 of this data sheet.

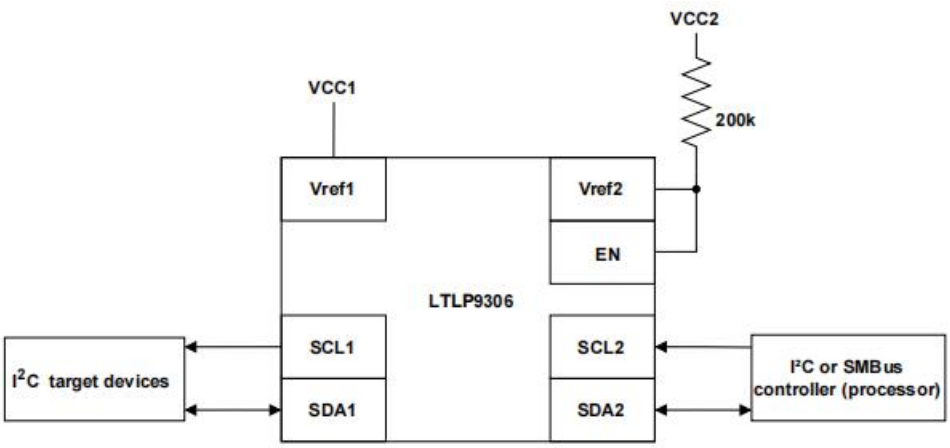


Figure 9:Controller on side 2 of LTLP9306

Detailed Description (Cont.)

LDO and LTLP9306 Concerns

The V_{REF1} pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO may lose its regulation because of the bias current from V_{REF2} to V_{REF1}. If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the V_{REF1} node (both external and parasitic). This results in an increase in voltage on the V_{REF1} node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the V_{REF1} node), then the V_{REF1} voltage ends up stabilizing when V_{gs} of the pass FET is equal to V_{th}. This means V_{REF1} node voltage is V_{CC2} - V_{th}. Note that any targets/controllers running off of the LDO now see the V_{CC2} - V_{th} voltage which may cause damage to those targets/controllers if they are not rated to handle the increased voltage.

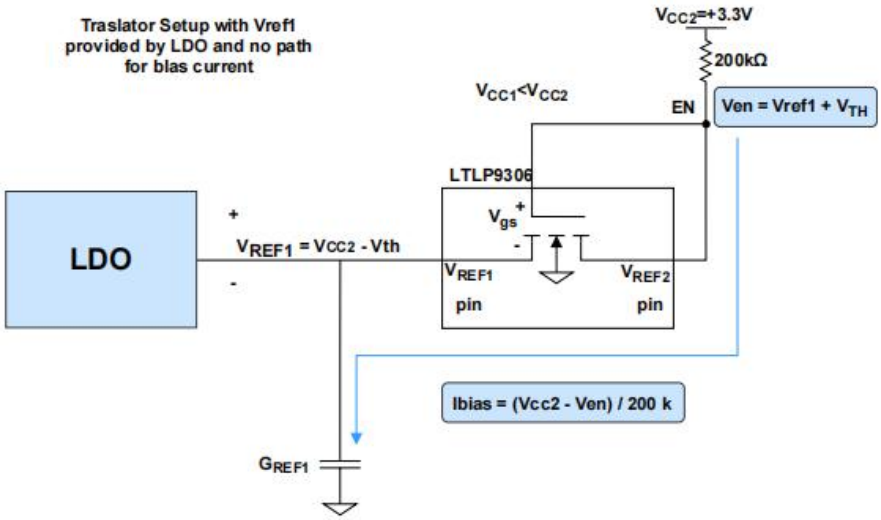


Figure 10:Example of no leakage current path when using LDO

To make sure the LDO does not lose regulation due to the bias current of LTLP9306, a weak pull down resistor can be placed on V_{REF1} to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by Equation 4 where 0.75 gives about 25% margin for error in case bias current increases during operation.

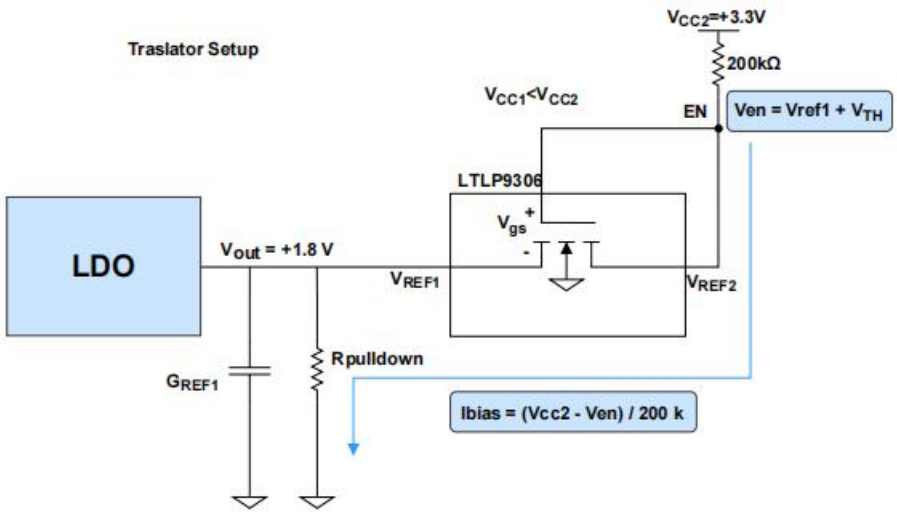


Figure 11:Example with Leakage current path when using an LDO

Detailed Description (Cont.)

$$V_{en} = V_{REF1} + V_{th} \quad (1)$$

where V_{th} is approximately 0.6V.

$$I_{bias} = \frac{V_{CC2} - V_{en}}{200k} \quad (2)$$

$$R_{pulldown} = V_{OUT}/I_{bias} \quad (3)$$

$$Recommended R_{pulldown} = R_{pulldown} \times 0.75 \quad (4)$$

Current Limiting Resistance on V_{REF2}

The resistor is used to limit the current between V_{REF2} and V_{REF1} (denoted as RCC) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value; however, the bias current proportionally increases as the resistor decreases.

$$I_{bias} = \frac{V_{CC2} - V_{en}}{R_{CC}} : V_{en} = V_{REF1} + V_{th} \quad (5)$$

where V_{th} is approximately 0.6V.

Keep in mind RCC should not be sized low enough that ICC exceeds the absolute maximum continuous channel current

specified in section 6.1 which is described in equation 6.

$$R_{CC}(min) \geq \frac{V_{CC2} - V_{en}}{0.128} : V_{en} = V_{REF1} + V_{th} \quad (6)$$

where Vth is approximately 0.6V.

Functional Block Diagram

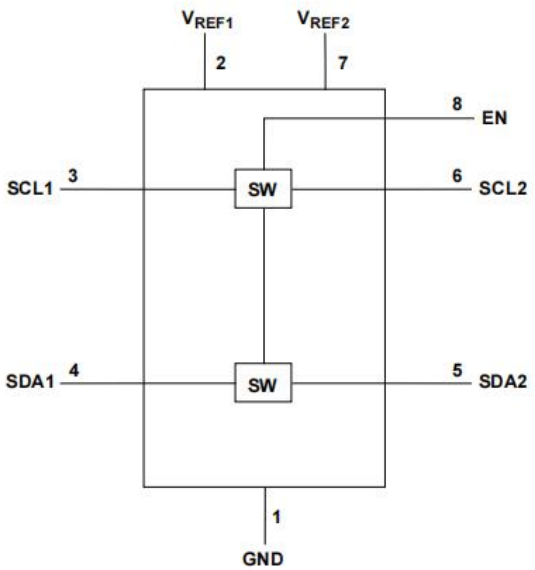


Figure 12:Block Diagram of LTLP9306

Detailed Description (Cont.)

Feature Description

Enable (EN) Pin

The LTLP9306 device is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In figure 13, the LTLP9306 device is always enabled when power is applied to V_{REF2}. In figure 14, the device is enabled when a control signal from a processor is in a logic-high state.

Voltage Translation

The primary feature of the LTLP9306 device is translating voltage from an I²C bus referenced to V_{REF1} up to an I²C bus referenced to V_{DPU} to which V_{REF2} is connected through a 200kΩ pullup resistor. Translation on a standard, open-drain I²C bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to V_{REF1} and connecting pullup resistors from SCL2 and SDA2 to V_{DPU}. Information on sizing the pullup resistors can be found in the Sizing Pullup Resistors section.

Application and Implementation

Application Information

General Applications of I²C

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I²C devices in addition to SMBus devices. Standard-mode I²C devices only specify 3mA in a generic I²C system where standard-mode devices and multiple controllers are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain (V_{DPU}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

Typical Application

The figure 13 and figure 14 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

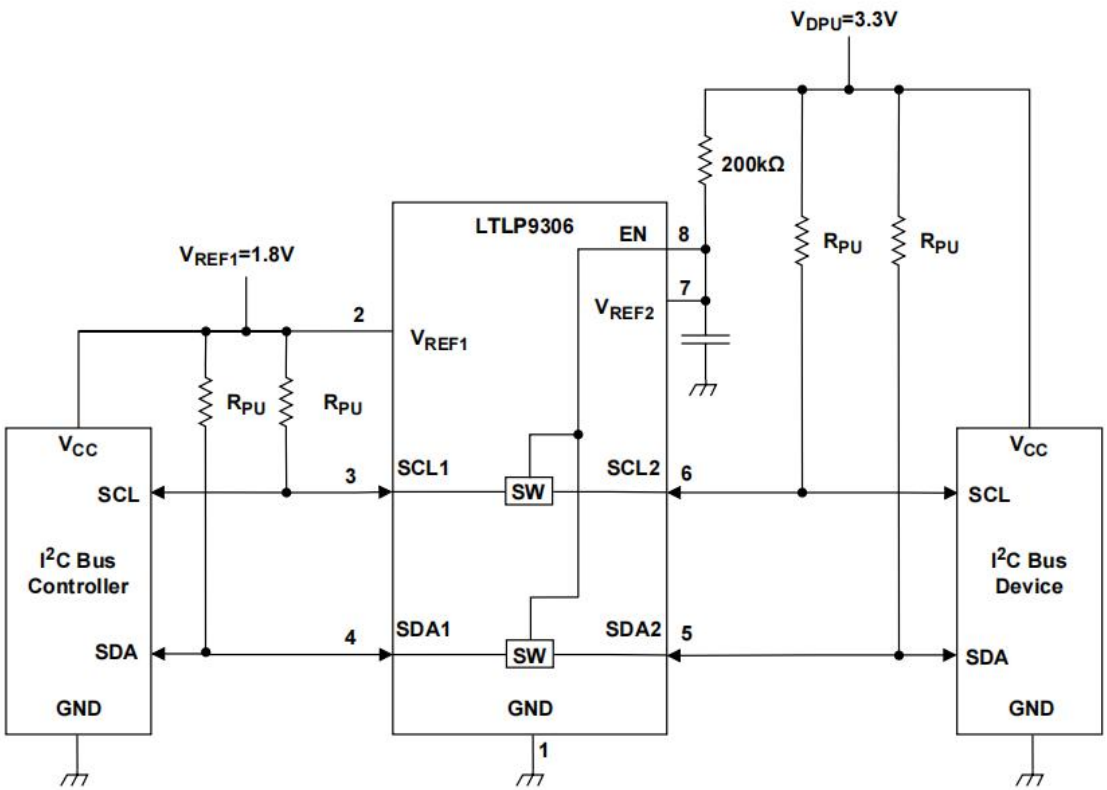


Figure 13:Typical Application Circuit (Switch Always Enabled)

Application and Implementation (Cont.)

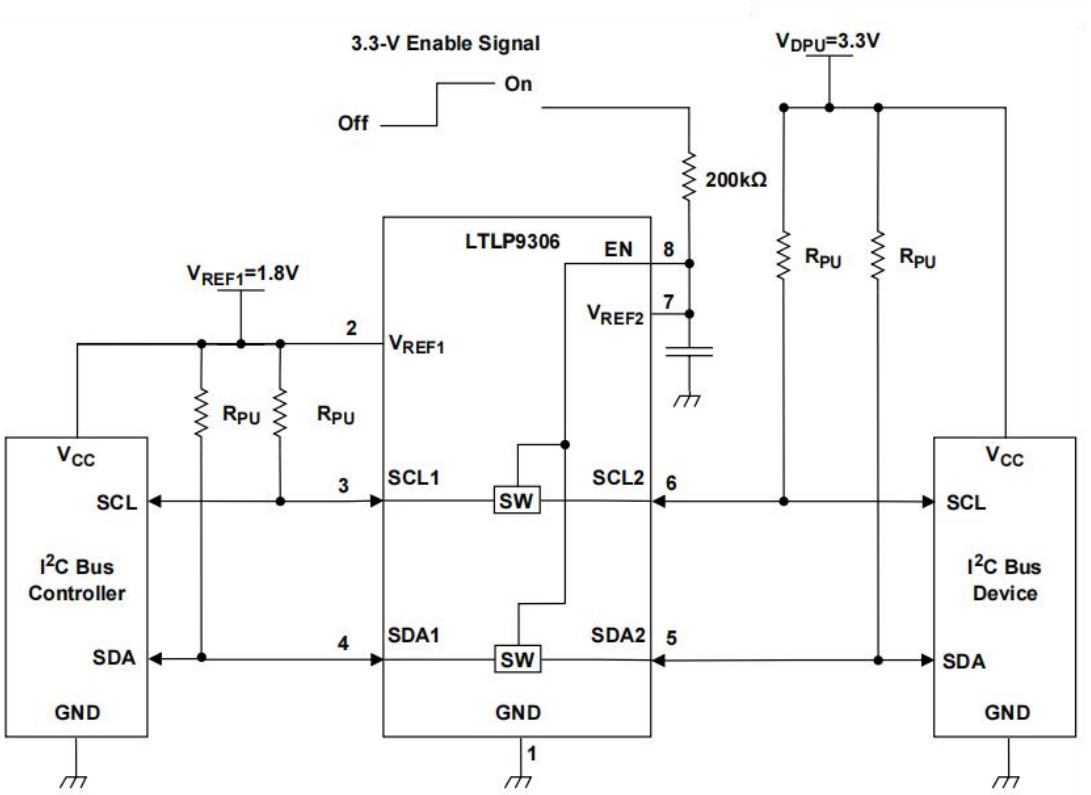


Figure 14:Typical Application Circuit (Switch Enable Control)

Design Requirements

Symbol	Parameter	MIN	TYP	MAX	UNIT
V_{REF2}	Reference voltage	V_{REF1}+0.6	2.1	5	V
EN	Enable input voltage	V_{REF1}+0.6	2.1	5	V
V_{REF1}	Reference voltage	1.2	1.5	4.4	V
I_{PASS}	Pass switch current		6		mA
I_{REF}	Reference-transistor current		5		µA

All typical values are at T_A = 25°C.

Detailed Design Procedure

Bidirectional Voltage Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200kΩ). This allows V_{REF2} to regulate the EN input. A 100pF filter capacitor connected to V_{REF2} is recommended. The I²C bus controller output can be push-pull or open-drain (pullup resistors may be required) and the I²C bus device output can be open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

Application and Implementation (Cont.)

Sizing Pullup Resistors

The figure 15 and figure 16 respectively show the maximum and minimum pullup resistance allowable by the I²C specification for standard-mode (100kHz) and fast-mode (400kHz) operation.

Application Curve

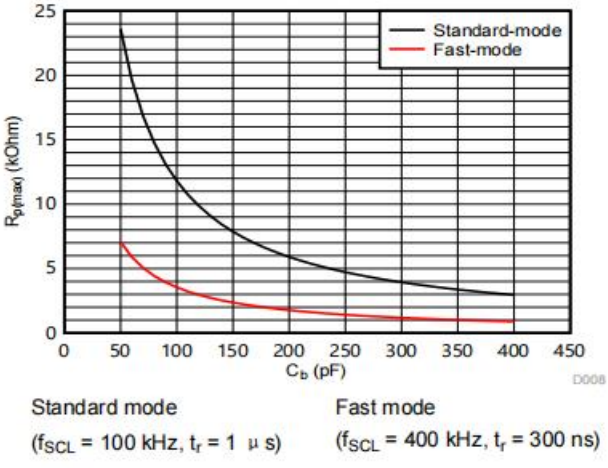


Figure 15:Maximum Pullup Resistance (Rp(max)) vs Bus Capacitance (Cb)

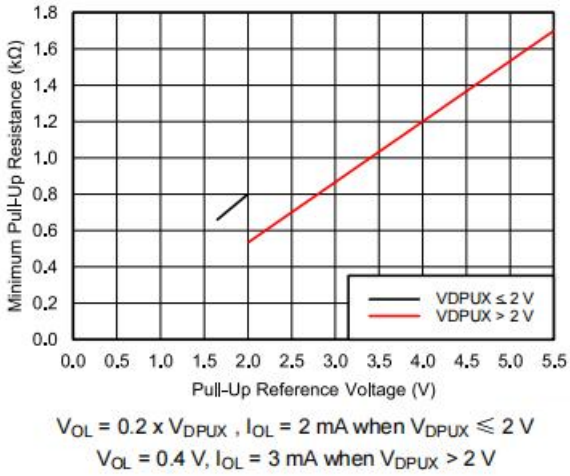


Figure 16:Minimum Pullup Resistance (Rp(min)) vs Pullup Reference Voltage (VDPUX)

Power Supply Recommendations

For supplying power to the LTLP9306 device, the V_{REF1} pin can be connected directly to a power supply. The V_{REF2} pin must be connected to the V_{DPU} power supply through a 200-kΩ resistor. Failure to have a high-impedance resistor between V_{REF2} and V_{DPU} results in excessive current draw and unreliable device operation. It is also worth noting, that in order to support voltage translation, the LTLP9306 must have the EN and V_{REF2} pins shorted and then pulled up to V_{DPU} through a high-impedance resistor.

Layout

Layout Guidelines

For printed-circuit board (PCB) layout of the LTLP9306 device, common PCB layout practices should be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other on leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor should be placed as close to V_{REF2} as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-k resistor results in longer turnon and turnoff times for the LTLP9306 device. These best practices are shown in figure 17.

For the layout example provided in figure 17, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to VCC or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in figure 17.

Application and Implementation (Cont.)

Layout Example

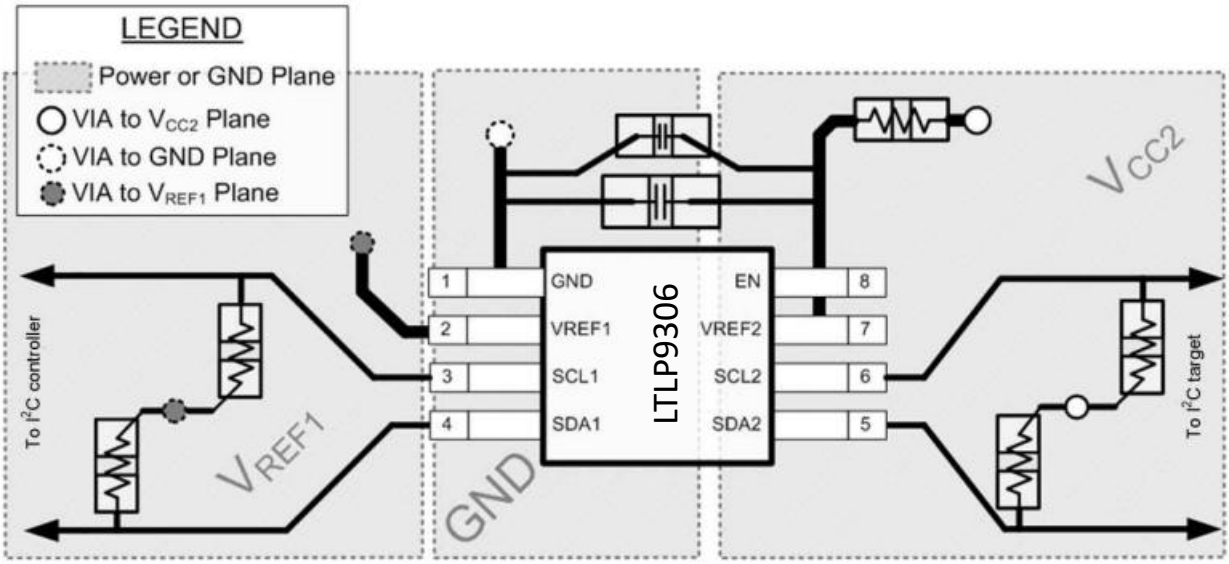
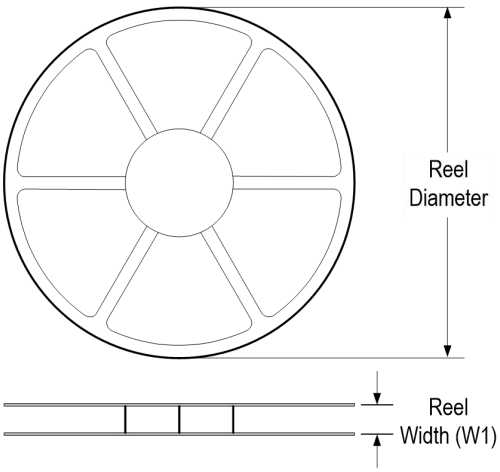


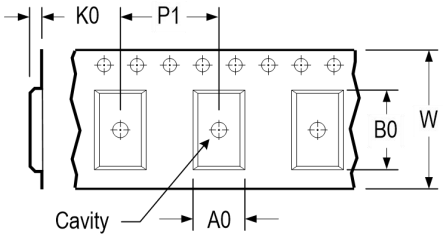
Figure 17:LTLP9306 Layout Example

Tape and Reel Information

REEL DIMENSIONS

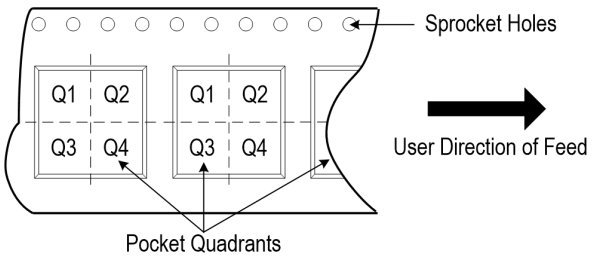


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

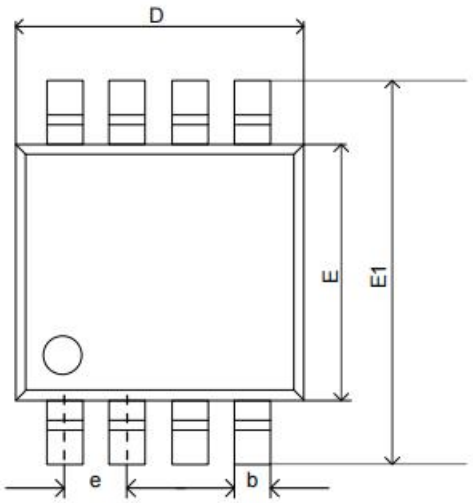


* All dimensions are nominal

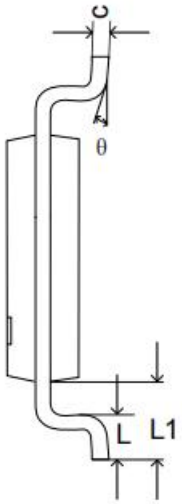
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTLP9306YV8/R6	MSOP	8	3 000	330	12.5	5.0	3.5	2.0	8.0	12.0	Q1
LTLP9306YF8/R6	DFN2x3	8	3 000	178	9.5	2.25	2.25	1.0	4.0	8.0	Q1

Package Dimension

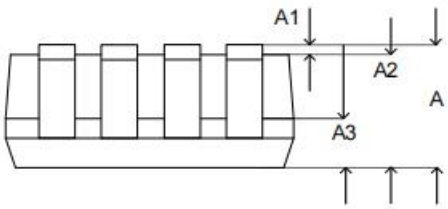
MSOP-8L



TOP VIEW



SIDE VIEW

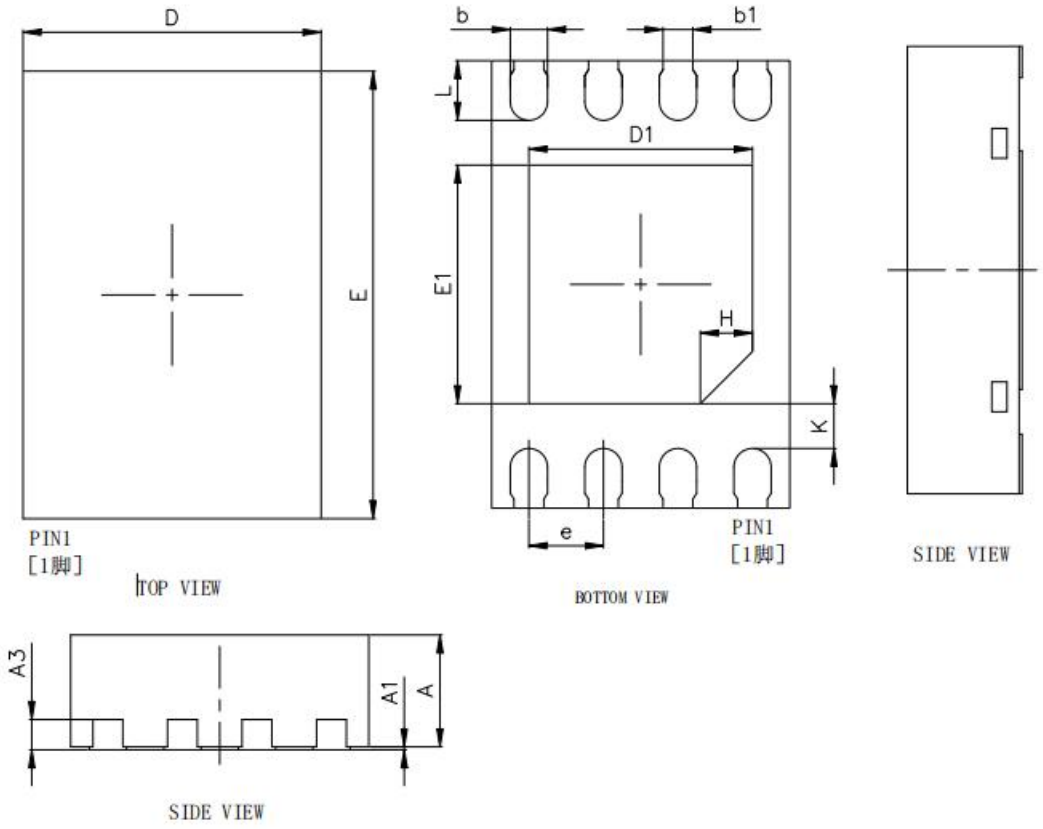


SIDE VIEW

SYMBOL	DIMENSIONS IN MILLIMETERS			SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX		MIN	NOM	MAX
A	-	-	1.10	E	2.90	3.00	3.10
A1	0.05	-	0.15	E1	4.70	4.90	5.10
A2	0.75	0.85	0.95	e		0.65BSC	
A3	0.30	0.35	0.40	L	0.40	-	0.70
b	0.28	-	0.36	L1		0.95REF	
c	0.15	-	0.19	θ	0°	-	8°
D	2.90	3.00	3.10				

Package Dimension (Cont.)

DFN2x3-8L



SYMBOL	DIMENSIONS IN MILLIMETERS			SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.700	0.750	0.800	E	2.900	3.000	3.100
A1	0.000	0.025	0.050	D1	1.400	1.500	1.600
A3		0.203REF		E1	2.900	3.000	3.100
D	1.900	2.000	2.100	K	0.250	0.300	0.350
b	0.200	0.250	0.300	b1	0.150	0.200	0.250
e		0.500REF		H		0.200REF	
L	0.300	0.400	0.500				

Important Notice

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