# LT74LVC1T45

Dual supply translating transceiver;3-State



## General Description

The LT74LVC1T45/LT74LVCH1T45 are single bit, dual supply transceivers with 3-state outputs that enable bidirectional level translation. They feature two 1-bit input-output ports (A and B), a direction control input (DIR) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2 V and 5.5 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins A and DIR are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from A to B and a LOW on DIR allows transmission from B to A.

The devices are fully specified for partial power-down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the LT74LVCH1T45 holds unused or floating data inputs at a valid logic level.

## Features and Benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2 V to 5.5 V
  - $V_{CC(B)}$: 1.2 V to 5.5 V
- High noise immunity
- Maximum data rates:
  - 420 Mbps (3.3 V to 5.0 V translation)
  - 210 Mbps (translate to 3.3 V)
  - 140 Mbps (translate to 2.5 V)
  - 75 Mbps (translate to 1.8 V)
  - 60 Mbps (translate to 1.5 V)
- Suspend mode
- ±24 mA output drive ($V_{CC}$ = 3.0 V)
- Inputs accept voltages up to 5.5 V
- Low power consumption: 16 µA maximum $I_{CC}$
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Complies with JEDEC standards
- Multiple package options：SOT23-6L/SC70-6L
- Specified from -40 °C to +125 °C

## Block Diagram and Pin Description

### Block Diagram

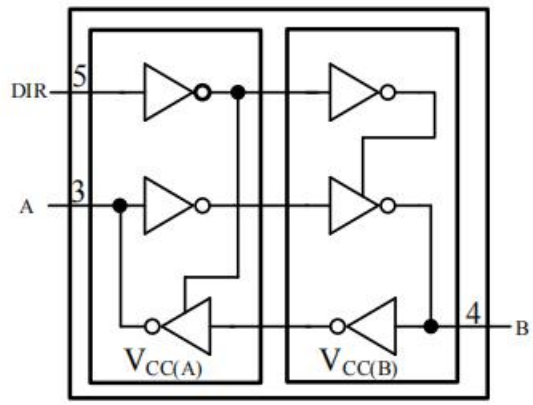



Figure 1. Logic symbol

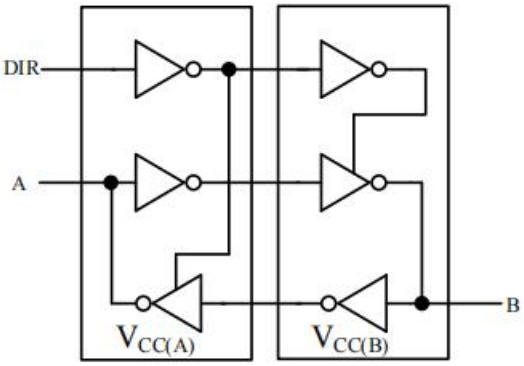
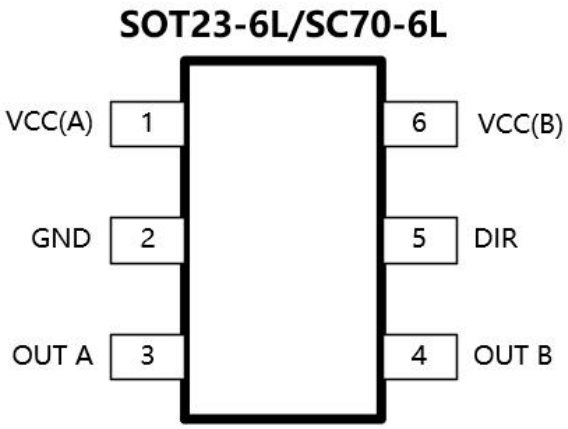



Figure 2. Logic diagram

### Pin Configurations




| Symbol | Pin No. | Function |
|---|---|---|
| $V_{CC(A)}$ | 1 | supply voltage A (port A and DIR). |
| GND | 2 | ground (0V). |
| OUT A | 3 | data input or output. |
| OUT B | 4 | data input or output. |
| DIR | 5 | direction control. |
| $V_{CC(B)}$ | 6 | supply voltage B (port B). |

## Ordering Information

| Package Type | Part Number | Quantity | Mark Code |
|---|---|---|---|
| SOT23-6L | LT74LVC1T45XT6/R6 | Tape and Reel, 3 000 | 1T45XX |
| SC70-6L | LT74LVC1T45XC6/R6 | Tape and Reel, 3 000 | 1T45XX |
| SOT23-6L | LT74LVCH1T45XT6/R6 | Tape and Reel, 3 000 | 1T45XX |
| SC70-6L | LT74LVCH1T45XC6/R6 | Tape and Reel, 3 000 | 1T45XX |

## Function Table

| Supply Voltage | Input | Input/Output | |
|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | DIR | A | B |
| 1.2V to 5.5V | L | A=B | input |
| 1.2V to 5.5V | H | input | B=A |
| GND | X | Z | Z |

Note:
[1]H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.
[2]The input circuit of the data I/O is always active.
[3]When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

## Electrical Parameter

### Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified).

| Characteristic | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| supply voltage A | $V_{CC(A)}$ | | -0.5 | +6.5 | V |
| supply voltage B | $V_{CC(B)}$ | | -0.5 | +6.5 | V |
| input clamping current | $I_{IK}$ | $V_I$<0V | -50 | | mA |
| input voltage | $V_I$ | | -0.5 | +6.5 | V |
| output clamping current | $I_{OK}$ | $V_O$<0V | -50 | | mA |
| output voltage | $V_O$ | Active mode | -0.5 | $V_{CCO}$+0.5 | v |
| | | Suspend or 3-state mode | -0.5 | +6.5 | v |
| output current | $I_O$ | $V_O$=0V to $V_{CCO}$ | | ±50 | mA |
| supply current | $I_{CC}$ | $I_{CC(A)}$ or $I_{CC(B)}$ | | 100 | mA |
| ground current | $I_{GND}$ | | -100 | | mA |
| storage temperature | $T_{stg}$ | | -65 | +150 | ℃ |
| total power dissipation | $P_{tot}$ | | | 250 | mW |
| soldering temperature | $T_L$ | 10s | | 260 | ℃ |

Note:
[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] $V_{CCO}$ is the supply voltage associated with the output port.
[3] $V_{CCO}$+0.5V should not exceed 6.5V.

## Electrical Parameter (Cont.)

### Recommended Operating Conditions

| Characteristic | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage A | $V_{CC(A)}$ | | 1.2 | 5.5 | V |
| Supply voltage B | $V_{CC(B)}$ | | 1.2 | 5.5 | V |
| Input voltage | $V_I$ | | 0 | 5.5 | V |
| Output voltage | $V_O$ | Active mode | 0 | $V_{CCO}$ | v |
| | | Suspend or 3-state mode | 0 | 5.5 | v |
| Ambient temperature | $T_{amb}$ | | -40 | +125 | ℃ |
| Input transition rise and fall rate | Δt/ΔV | $V_{CCI}$=1.2V | | 20 | ns/V |
| | | $V_{CCI}$=1.4V to 1.95V | | 20 | ns/V |
| | | $V_{CCI}$=2.3V to 2.7V | | 20 | ns/V |
| | | $V_{CCI}$=3V to 3.6V | | 10 | ns/V |
| | | $V_{CCI}$=4.5V to 5.5V | | 5 | ns/V |

Note:
[1] $V_{CCO}$ is the supply voltage associated with the output port.
[2] $V_{CCI}$ is the supply voltage associated with the input port.

## Electrical Characteristics

### DC Characteristics 1

Tamb=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| HIGH-level output voltage | $V_{OH}$ | $V_I$=$V_{IH}$ or $V_{IL}$; $I_O$=-3mA; $V_{CCO}$=1.2V | | 1.09 | | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$=$V_{IH}$ or $V_{IL}$; $I_O$=3mA; $V_{CCO}$=1.2V | | 0.07 | | V |
| Input leakage current | $I_I$ | DIR input; $V_I$=0V to 5.5V; $V_{CCI}$=1.2V to 5.5V | | | ±1 | μA |
| Bus hold LOW current | $I_{BHL}$ | A or B port; $V_I$=0.42V; $V_{CCI}$=1.2V | | 19 | | μA |
| Bus hold HIGH current | $I_{BHH}$ | A or B port; $V_I$=0.78V; $V_{CCI}$=1.2V | | -19 | | μA |
| Bus hold LOW overdrive current | $I_{BHLO}$ | A or B port; $V_{CCI}$=1.2V | | 19 | | μA |
| Bus hold HIGH overdrive current | $I_{BHHO}$ | A or B port; $V_{CCI}$=1.2V | | -19 | | μA |
| OFF-state output current | $I_{OZ}$ | A or B port; $V_O$=0V or $V_{CCO}$; $V_{CCO}$=1.2V to 5.5V | | | ±1 | μA |
| Power-off leakage current | $I_{OFF}$ | A port; $V_I$ or $V_O$=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V | | | ±1 | μA |
| | | B port; $V_I$ or $V_O$=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V | | | ±1 | μA |
| Input capacitance | $C_I$ | DIR input; $V_I$=0V or 3.3V; $V_{CC(A)}$=$V_{CC(B)}$=3.3V | | 2.2 | | pF |
| Input/output capacitance | $C_{I/O}$ | A and B port; suspend mode; $V_O$=3.3V or 0V; $V_{CC(A)}$=$V_{CC(B)}$=3.3V | | 6.0 | | pF |

Note:
[1] $V_{CCO}$ is the supply voltage associated with the output port.
[2] $V_{CCI}$ is the supply voltage associated with the data input port.
[3] To guarantee the node switches, an external driver must source/sink at least $I_{BHLO}$/$I_{BHHO}$ when the input is in the range $V_{IL}$ to $V_{IH}$.

## Electrical Characteristics (Cont.)

### DC Characteristics 2

Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | Data input | $V_{CCI}$=1.2V | 0.8$V_{CCI}$ | | | V |
| | | | $V_{CCI}$=1.4V to 1.95V | 0.65$V_{CCI}$ | | | V |
| | | | $V_{CCI}$=2.3V to 2.7V | 1.7 | | | V |
| | | | $V_{CCI}$=3.0V to 3.6V | 2.0 | | | V |
| | | | $V_{CCI}$=4.5V to 5.5V | 0.7$V_{CCI}$ | | | V |
| | | DIR input | $V_{CCI}$=1.2V | 0.8$V_{CC}$(A) | | | V |
| | | | $V_{CCI}$=1.4V to 1.95V | 0.65$V_{CC}$(A) | | | V |
| | | | $V_{CCI}$=2.3V to 2.7V | 1.7 | | | V |
| | | | $V_{CCI}$=3.0V to 3.6V | 2.0 | | | V |
| | | | $V_{CCI}$=4.5V to 5.5V | 0.7$V_{CC}$(A) | | | V |
| LOW-level input voltage | $V_{IL}$ | Data input | $V_{CCI}$=1.2V | | | 0.2$V_{CCI}$ | V |
| | | | $V_{CCI}$=1.4V to 1.95V | | | 0.35$V_{CCI}$ | V |
| | | | $V_{CCI}$=2.3V to 2.7V | | | 0.7 | V |
| | | | $V_{CCI}$=3.0V to 3.6V | | | 0.8 | V |
| | | | $V_{CCI}$=4.5V to 5.5V | | | 0.3$V_{CCI}$ | V |
| | | DIR input | $V_{CCI}$=1.2V | | | 0.2$V_{CC}$(A) | V |
| | | | $V_{CCI}$=1.4V to 1.95V | | | 0.35$V_{CC}$(A) | V |
| | | | $V_{CCI}$=2.3V to 2.7V | | | 0.7 | V |
| | | | $V_{CCI}$=3.0V to 3.6V | | | 0.8 | V |
| | | | $V_{CCI}$=4.5V to 5.5V | | | 0.3$V_{CC}$(A) | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$=$V_{IH}$ | $I_O$=-100uA; $V_{CCO}$=1.2V to 4.5V | $V_{CCO}$-0.1 | | | V |
| | | | $I_O$=-6mA; $V_{CCO}$=1.4V | 1.0 | | | V |
| | | | $I_O$=-8mA; $V_{CCO}$=1.65V | 1.2 | | | V |
| | | | $I_O$=-12mA; $V_{CCO}$=2.3V | 1.9 | | | V |
| | | | $I_O$=-24mA; $V_{CCO}$=3.0V | 2.4 | | | V |
| | | | $I_O$=-32mA; $V_{CCO}$=4.5V | 3.8 | | | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$=$V_{IL}$ | $I_O$=100uA; $V_{CCO}$=1.2V to 4.5V | | | 0.1 | V |
| | | | $I_O$=6mA; $V_{CCO}$=1.4V | | | 0.3 | V |
| | | | $I_O$=8mA; $V_{CCO}$=1.65V | | | 0.45 | V |
| | | | $I_O$=12mA; $V_{CCO}$=2.3V | | | 0.3 | V |
| | | | $I_O$=24mA; $V_{CCO}$=3.0V | | | 0.55 | V |

## Electrical Characteristics (Cont.)

### DC Characteristics 2

Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| LOW-level output voltage | $V_{OL}$ | $V_I=V_{IL}$ | $I_O$=32mA; $V_{CCO}$=4.5V | | | 0.55 | V |
| Input leakage current | $I_I$ | DIR input; $V_I$=0V to 5.5V; $V_{CCI}$=1.2V to 5.5V | | | | ±2 | μA |
| Bus hold LOW current | $I_{BHL}$ | A or B port | $V_I$=0.49V; $V_{CCI}$=1.4V | 15 | | | μA |
| | | | $V_I$=0.58V; $V_{CCI}$=1.65V | 25 | | | μA |
| | | | $V_I$=0.70V; $V_{CCI}$=2.3V | 45 | | | μA |
| | | | $V_I$=0.80V; $V_{CCI}$=3.0V | 100 | | | μA |
| | | | $V_I$=1.35V; $V_{CCI}$=4.5V | 100 | | | μA |
| Bus hold HIGH current | $I_{BHH}$ | A or B port | $V_I$=0.91V; $V_{CCI}$=1.4V | -15 | | | μA |
| | | | $V_I$=1.07V; $V_{CCI}$=1.65V | -25 | | | μA |
| | | | $V_I$=1.60V; $V_{CCI}$=2.3V | -45 | | | μA |
| | | | $V_I$=2.00V; $V_{CCI}$=3.0V | -100 | | | μA |
| | | | $V_I$=3.15V; $V_{CCI}$=4.5V | -100 | | | μA |
| Bus hold LOW overdrive current | $I_{BHLO}$ | A or B port | $V_{CCI}$=1.6V | 125 | | | μA |
| | | | $V_{CCI}$=1.95V | 200 | | | μA |
| | | | $V_{CCI}$=2.7V | 300 | | | μA |
| | | | $V_{CCI}$=3.6V | 500 | | | μA |
| | | | $V_{CCI}$=5.5V | 900 | | | μA |
| bus hold HIGH overdrive current | $I_{BHHO}$ | A or B port | $V_{CCI}$=1.6V | -125 | | | μA |
| | | | $V_{CCI}$=1.95V | -200 | | | μA |
| | | | $V_{CCI}$=2.7V | -300 | | | μA |
| | | | $V_{CCI}$=3.6V | -500 | | | μA |
| | | | $V_{CCI}$=5.5V | -900 | | | μA |
| OFF-state output | $I_{OZ}$ | A or B port; $V_O$=0V or $V_{CCO}$; $V_{CCO}$=1.2V to 5.5V | | | | ±2 | μA |
| Power-off leakage current | $I_{OFF}$ | A port; $V_I$ or $V_O$=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V | | | | ±2 | μA |
| | | B port; $V_I$ or $V_O$=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V | | | | ±2 | μA |
| Supply current | $I_{CC}$ | A port; $V_I$=0V or $V_{CCI}$; $I_O$=0A | $V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V | | | 8 | μA |
| | | | $V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V | | | 3 | μA |
| | | | $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V | | | 2 | μA |
| | | | $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V | -2 | | | μA |

## Electrical Characteristics (Cont.)

### DC Characteristics 2

Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply current | $I_{CC}$ | B port; $V_I$=0V or $V_{CCI}$; $I_O$=0A | $V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V | | | 8 | μA |
| | | | $V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V | | | 3 | μA |
| | | | $V_{CC(B)}$=0V; $V_{CC(A)}$=5.5V | -2 | | | μA |
| | | | $V_{CC(B)}$=5.5V; $V_{CC(A)}$=0V | | | 2 | μA |
| | | A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); $I_O$=0A; $V_I$=0V or $V_{CCI}$ | $V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V | | | 16 | μA |
| | | | $V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V | | | 4 | μA |
| Additional supply current | $\Delta_{ICC}$ | per input; $V_{CC(A)}$, $V_{CC(B)}$= 3.0V to 5.5V | A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open | | | 50 | μA |
| | | | DIR input; DIR at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open | | | 50 | μA |
| | | | B port; B port at $V_{CC(B)}$-0.6V; DIR at GND; A port=open | | | 50 | μA |

Note:
[1] $V_{CCI}$ is the supply voltage associated with the data input port.
[2] $V_{CCO}$ is the supply voltage associated with the output port.
[3] To guarantee the node switches, an external driver must source/sink at least $I_{BHLO}$/$I_{BHHO}$ when the input is in the range $V_{IL}$ to $V_{IH}$.
[4] For non bus hold parts only (LT74LVC1T45).

## Electrical Characteristics (Cont.)

### DC Characteristics 3

Tamb=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| LOW-level output voltage | $V_{OL}$ | $V_I=V_{IL}$ | $I_O$=32mA; $V_{CCO}$=4.5V | | | 0.55 | V |
| Input leakage current | $I_I$ | DIR input; $V_I$=0V to 5.5V; $V_{CCI}$=1.2V to 5.5V | | | | ±2 | μA |
| Bus hold LOW current | $I_{BHL}$ | A or B port | $V_I$=0.49V; $V_{CCI}$=1.4V | 10 | | | μA |
| | | | $V_I$=0.58V; $V_{CCI}$=1.65V | 20 | | | μA |
| | | | $V_I$=0.70V; $V_{CCI}$=2.3V | 45 | | | μA |
| | | | $V_I$=0.80V; $V_{CCI}$=3.0V | 80 | | | μA |
| | | | $V_I$=1.35V; $V_{CCI}$=4.5V | 100 | | | μA |
| Bus hold HIGH current | $I_{BHH}$ | A or B port | $V_I$=0.91V; $V_{CCI}$=1.4V | -10 | | | μA |
| | | | $V_I$=1.07V; $V_{CCI}$=1.65V | -20 | | | μA |
| | | | $V_I$=1.60V; $V_{CCI}$=2.3V | -45 | | | μA |
| | | | $V_I$=2.00V; $V_{CCI}$=3.0V | -80 | | | μA |
| | | | $V_I$=3.15V; $V_{CCI}$=4.5V | -100 | | | μA |
| Bus hold LOW overdrive current | $I_{BHLO}$ | A or B port | $V_{CCI}$=1.6V | 125 | | | μA |
| | | | $V_{CCI}$=1.95V | 200 | | | μA |
| | | | $V_{CCI}$=2.7V | 300 | | | μA |
| | | | $V_{CCI}$=3.6V | 500 | | | μA |
| | | | $V_{CCI}$=5.5V | 900 | | | μA |
| bus hold HIGH overdrive current | $I_{BHHO}$ | A or B port | $V_{CCI}$=1.6V | -125 | | | μA |
| | | | $V_{CCI}$=1.95V | -200 | | | μA |
| | | | $V_{CCI}$=2.7V | -300 | | | μA |
| | | | $V_{CCI}$=3.6V | -500 | | | μA |
| | | | $V_{CCI}$=5.5V | -900 | | | μA |
| OFF-state output | $I_{OZ}$ | A or B port; $V_O$=0V or $V_{CCO}$; $V_{CCO}$=1.2V to 5.5V | | | | ±10 | μA |
| Power-off leakage current | $I_{OFF}$ | A port; $V_I$ or $V_O$=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V | | | | ±10 | μA |
| | | B port; $V_I$ or $V_O$=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V | | | | ±10 | μA |
| Supply current | $I_{CC}$ | A port; $V_I$=0V or $V_{CCI}$; $I_O$=0A | $V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V | | | 8 | μA |
| | | | $V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V | | | 3 | μA |
| | | | $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V | | | 2 | μA |
| | | | $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V | -2 | | | μA |

## Electrical Characteristics (Cont.)

### DC Characteristics 3

Tamb=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | Data input | $V_{CCI}$=1.2V | 0.8$V_{CCI}$ | | | V |
| | | | $V_{CCI}$=1.4V to 1.95V | 0.65$V_{CCI}$ | | | V |
| | | | $V_{CCI}$=2.3V to 2.7V | 1.7 | | | V |
| | | | $V_{CCI}$=3.0V to 3.6V | 2.0 | | | V |
| | | | $V_{CCI}$=4.5V to 5.5V | 0.7$V_{CCI}$ | | | V |
| | | DIR input | $V_{CCI}$=1.2V | 0.8$V_{CC}$(A) | | | V |
| | | | $V_{CCI}$=1.4V to 1.95V | 0.65$V_{CC}$(A) | | | V |
| | | | $V_{CCI}$=2.3V to 2.7V | 1.7 | | | V |
| | | | $V_{CCI}$=3.0V to 3.6V | 2.0 | | | V |
| | | | $V_{CCI}$=4.5V to 5.5V | 0.7$V_{CC}$(A) | | | V |
| LOW-level input voltage | $V_{IL}$ | Data input | $V_{CCI}$=1.2V | | | 0.2$V_{CCI}$ | V |
| | | | $V_{CCI}$=1.4V to 1.95V | | | 0.35$V_{CCI}$ | V |
| | | | $V_{CCI}$=2.3V to 2.7V | | | 0.7 | V |
| | | | $V_{CCI}$=3.0V to 3.6V | | | 0.8 | V |
| | | | $V_{CCI}$=4.5V to 5.5V | | | 0.3$V_{CCI}$ | V |
| | | DIR input | $V_{CCI}$=1.2V | | | 0.2$V_{CC}$(A) | V |
| | | | $V_{CCI}$=1.4V to 1.95V | | | 0.35$V_{CC}$(A) | V |
| | | | $V_{CCI}$=2.3V to 2.7V | | | 0.7 | V |
| | | | $V_{CCI}$=3.0V to 3.6V | | | 0.8 | V |
| | | | $V_{CCI}$=4.5V to 5.5V | | | 0.3$V_{CC}$(A) | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$=$V_{IH}$ | $I_O$=-100uA; $V_{CCO}$=1.2V to 4.5V | $V_{CCO}$-0.1 | | | V |
| | | | $I_O$=-6mA; $V_{CCO}$=1.4V | 1.0 | | | V |
| | | | $I_O$=-8mA; $V_{CCO}$=1.65V | 1.2 | | | V |
| | | | $I_O$=-12mA; $V_{CCO}$=2.3V | 1.9 | | | V |
| | | | $I_O$=-24mA; $V_{CCO}$=3.0V | 2.4 | | | V |
| | | | $I_O$=-32mA; $V_{CCO}$=4.5V | 3.8 | | | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$=$V_{IL}$ | $I_O$=100uA; $V_{CCO}$=1.2V to 4.5V | | | 0.1 | V |
| | | | $I_O$=6mA; $V_{CCO}$=1.4V | | | 0.3 | V |
| | | | $I_O$=8mA; $V_{CCO}$=1.65V | | | 0.45 | V |
| | | | $I_O$=12mA; $V_{CCO}$=2.3V | | | 0.3 | V |
| | | | $I_O$=24mA; $V_{CCO}$=3.0V | | | 0.55 | V |

## Electrical Characteristics (Cont.)

### DC Characteristics 3

Tamb=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply current | $I_{CC}$ | B port; $V_I$=0V or $V_{CCI}$; $I_O$=0A | $V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V | | | 8 | μA |
| | | | $V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V | | | 3 | μA |
| | | | $V_{CC(B)}$=0V; $V_{CC(A)}$=5.5V | -2 | | | μA |
| | | | $V_{CC(B)}$=5.5V; $V_{CC(A)}$=0V | | | 2 | μA |
| | | A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); $I_O$=0A; $V_I$=0V or $V_{CCI}$ | $V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V | | | 16 | μA |
| | | | $V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V | | | 4 | μA |
| Additional supply current | $\Delta_{ICC}$ | per input; $V_{CC(A)}$, $V_{CC(B)}$= 3.0V to 5.5V | A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open | | | 75 | μA |
| | | | DIR input; DIR at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open | | | 75 | μA |
| | | | B port; B port at $V_{CC(B)}$-0.6V; DIR at GND; A port=open | | | 75 | μA |

Note:
[1] $V_{CCI}$ is the supply voltage associated with the data input port.
[2] $V_{CCO}$ is the supply voltage associated with the output port.
[3] To guarantee the node switches, an external driver must source/sink at least $I_{BHLO}$/$I_{BHHO}$ when the input is in the range $V_{IL}$ to $V_{IH}$.
[4] For non bus hold parts only (LT74LVC1T45).

## Electrical Characteristics (Cont.)

### AC Characteristics 1

Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Conditions | VCC(B) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.5V±0.1V | | 1.8V±0.15V | | 2.5V±0.2V | | 3.3V±0.3V | | 5.0V±0.5V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $V_{CC(A)}$=1.4V to 1.6V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 22.0 | | 18.2 | | 13.7 | | 12.0 | | 10.7 | ns |
| | | B to A | | 22.0 | | 19.5 | | 16.2 | | 15.9 | | 15.5 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 19.7 | | 15.6 | | 12.1 | | 11.1 | | 10.8 | ns |
| | | B to A | | 19.7 | | 17.6 | | 13.5 | | 11.5 | | 11.2 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 19.2 | | 19.2 | | 19.2 | | 19.2 | | 19.2 | ns |
| | | DIR to B | | 25.0 | | 23.8 | | 14.1 | | 13.2 | | 12.5 | ns |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 11.7 | | 11.7 | | 11.7 | | 11.7 | | 11.7 | ns |
| | | DIR to B | | 18.5 | | 17.5 | | 13.2 | | 12.4 | | 11.6 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 39.7 | | 36.7 | | 24.8 | | 23.0 | | 21.8 | ns |
| | | DIR to B | | 33.0 | | 29.5 | | 25.3 | | 23.3 | | 22.3 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 44.5 | | 41.2 | | 24.6 | | 22.9 | | 21.6 | ns |
| | | DIR to B | | 38.3 | | 34.7 | | 31.1 | | 30.2 | | 29.8 | ns |
| $V_{CC(A)}$=1.65V to 1.95V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 19.5 | | 18.1 | | 9.7 | | 7.7 | | 7.2 | ns |
| | | B to A | | 18.3 | | 18.1 | | 15.2 | | 12.6 | | 12.2 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 17.4 | | 14.4 | | 9.0 | | 7.5 | | 7.3 | ns |
| | | B to A | | 15.6 | | 14.4 | | 13.2 | | 12.9 | | 12.5 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 17.5 | | 17.5 | | 17.5 | | 17.5 | | 17.5 | ns |
| | | DIR to B | | 24.5 | | 22.3 | | 12.8 | | 12.0 | | 10.5 | ns |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 11.1 | | 11.1 | | 11.1 | | 11.1 | | 11.1 | ns |
| | | DIR to B | | 18.4 | | 16.9 | | 11.3 | | 10.5 | | 9.5 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 35.6 | | 33.9 | | 25.6 | | 24.4 | | 22.3 | ns |
| | | DIR to B | | 30.0 | | 28.5 | | 20.3 | | 18.1 | | 17.5 | ns |

## Electrical Characteristics (Cont.)

### AC Characteristics 1

Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Conditions | VCC(B) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.5V±0.1V | | 1.8V±0.15V | | 2.5V±0.2V | | 3.3V±0.3V | | 5.0V±0.5V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 39.8 | | 36.5 | | 24.8 | | 23.3 | | 20.6 | ns |
| | | DIR to B | | 35.0 | | 31.9 | | 26.0 | | 24.6 | | 24.5 | ns |
| $V_{CC(A)}$=2.3V to 2.7V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 18.1 | | 16.1 | | 8.7 | | 6.5 | | 5.0 | ns |
| | | B to A | | 13.7 | | 9.2 | | 8.7 | | 7.8 | | 7.5 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 15.9 | | 13.2 | | 7.6 | | 5.9 | | 4.9 | ns |
| | | B to A | | 12.3 | | 8.7 | | 7.6 | | 7.0 | | 6.2 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 8.2 | | 8.2 | | 8.2 | | 8.2 | | 8.2 | ns |
| | | DIR to B | | 22.5 | | 21.6 | | 11.2 | | 9.2 | | 8.3 | ns |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 6.2 | | 6.2 | | 6.2 | | 6.2 | | 6.2 | ns |
| | | DIR to B | | 14.6 | | 13.3 | | 9.2 | | 8.7 | | 7.7 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 27.7 | | 22.3 | | 17.2 | | 16.5 | | 12.6 | ns |
| | | DIR to B | | 23.5 | | 21.5 | | 14.1 | | 11.9 | | 10.5 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 34.1 | | 29.5 | | 18.3 | | 16.2 | | 13.0 | ns |
| | | DIR to B | | 23.7 | | 20.9 | | 15.5 | | 13.5 | | 12.5 | ns |
| $V_{CC(A)}$=3.0V to 3.6V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 17.2 | | 15.5 | | 7.9 | | 5.6 | | 4.5 | ns |
| | | B to A | | 11.7 | | 7.3 | | 6.4 | | 5.6 | | 5.5 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 15.5 | | 12.5 | | 7.0 | | 5.0 | | 4.4 | ns |
| | | B to A | | 11.0 | | 7.2 | | 5.6 | | 5.0 | | 4.5 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 7.3 | | 7.3 | | 7.3 | | 7.3 | | 7.3 | ns |
| | | DIR to B | | 18.1 | | 16.6 | | 10.4 | | 8.7 | | 6.8 | ns |

## Electrical Characteristics (Cont.)

### AC Characteristics 1

Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Conditions | VCC(B) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.5V±0.1V | | 1.8V±0.15V | | 2.5V±0.2V | | 3.3V±0.3V | | 5.0V±0.5V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 5.8 | | 5.8 | | 5.8 | | 5.8 | | 5.8 | ns |
| | | DIR to B | | 13.8 | | 12.7 | | 8.0 | | 7.4 | | 6.8 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 25.0 | | 19.4 | | 13.8 | | 12.6 | | 10.0 | ns |
| | | DIR to B | | 22.5 | | 20.7 | | 13.3 | | 10.9 | | 9.8 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 28.5 | | 23.3 | | 15.3 | | 13.3 | | 10.5 | ns |
| | | DIR to B | | 22.7 | | 19.7 | | 14.1 | | 12.1 | | 11.1 | ns |
| $V_{CC(A)}$=4.5V to 5.5V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 16.5 | | 15.0 | | 7.7 | | 5.6 | | 3.9 | ns |
| | | B to A | | 10.4 | | 6.6 | | 5.0 | | 4.5 | | 3.9 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 15.0 | | 12.1 | | 6.3 | | 4.5 | | 3.6 | ns |
| | | B to A | | 10.4 | | 6.5 | | 4.6 | | 4.0 | | 3.6 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 5.5 | | 5.5 | | 5.5 | | 5.5 | | 5.5 | ns |
| | | DIR to B | | 16.9 | | 15.9 | | 9.5 | | 8.0 | | 6.5 | ns |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 5.3 | | 5.3 | | 5.3 | | 5.3 | | 5.3 | ns |
| | | DIR to B | | 13.0 | | 11.8 | | 7.5 | | 7.1 | | 6.5 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 23.5 | | 18.7 | | 12.0 | | 10.9 | | 8.3 | ns |
| | | DIR to B | | 20.0 | | 18.6 | | 11.0 | | 9.1 | | 7.4 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 27.7 | | 23.3 | | 14.1 | | 11.6 | | 9.3 | ns |
| | | DIR to B | | 20.5 | | 17.7 | | 11.3 | | 9.6 | | 8.9 | ns |

Note:
[1] $t_{PZH}$ and $t_{PZL}$ are calculated values using the formula shown in Section 9.4.

## Electrical Characteristics (Cont.)

### AC Characteristics 2

Tamb=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Conditions | VCC(B) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.5V±0.1V | | 1.8V±0.15V | | 2.5V±0.2V | | 3.3V±0.3V | | 5.0V±0.5V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $V_{CC(A)}$=1.4V to 1.6V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 24.2 | | 20.0 | | 15.1 | | 13.2 | | 11.8 | ns |
| | | B to A | | 24.2 | | 21.4 | | 17.8 | | 17.5 | | 17.1 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 21.7 | | 17.2 | | 13.3 | | 12.2 | | 11.9 | ns |
| | | B to A | | 21.7 | | 19.4 | | 14.9 | | 12.7 | | 12.3 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 21.1 | | 21.1 | | 21.1 | | 21.1 | | 21.1 | ns |
| | | DIR to B | | 27.5 | | 26.2 | | 15.5 | | 14.5 | | 13.8 | ns |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 12.9 | | 12.9 | | 12.9 | | 12.9 | | 12.9 | ns |
| | | DIR to B | | 20.4 | | 19.3 | | 14.5 | | 13.6 | | 12.8 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 43.7 | | 40.4 | | 27.3 | | 25.3 | | 24.0 | ns |
| | | DIR to B | | 36.3 | | 32.4 | | 27.8 | | 25.6 | | 24.5 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 48.9 | | 45.3 | | 27.1 | | 25.2 | | 23.8 | ns |
| | | DIR to B | | 42.1 | | 38.2 | | 34.2 | | 33.2 | | 32.8 | ns |
| $V_{CC(A)}$=1.65V to 1.95V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 21.4 | | 19.9 | | 10.7 | | 8.5 | | 7.9 | ns |
| | | B to A | | 20.1 | | 19.9 | | 16.7 | | 13.9 | | 13.4 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 19.1 | | 15.8 | | 9.9 | | 8.3 | | 8.0 | ns |
| | | B to A | | 17.2 | | 15.8 | | 14.5 | | 14.2 | | 13.7 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 19.2 | | 19.2 | | 19.2 | | 19.2 | | 19.2 | ns |
| | | DIR to B | | 26.9 | | 24.5 | | 14.1 | | 13.2 | | 11.5 | ns |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 12.2 | | 12.2 | | 12.2 | | 12.2 | | 12.2 | ns |
| | | DIR to B | | 20.2 | | 18.6 | | 12.4 | | 11.5 | | 10.4 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 39.2 | | 37.3 | | 28.2 | | 26.8 | | 24.5 | ns |
| | | DIR to B | | 33.0 | | 31.4 | | 22.3 | | 19.9 | | 19.3 | ns |

## Electrical Characteristics (Cont.)

### AC Characteristics 2

Tamb=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Conditions | VCC(B) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.5V±0.1V | | 1.8V±0.15V | | 2.5V±0.2V | | 3.3V±0.3V | | 5.0V±0.5V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 43.8 | | 40.2 | | 27.3 | | 25.6 | | 22.7 | ns |
| | | DIR to B | | 38.5 | | 35.1 | | 28.6 | | 27.1 | | 26.9 | ns |
| $V_{CC(A)}$=2.3V to 2.7V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 19.9 | | 17.7 | | 9.6 | | 7.1 | | 5.5 | ns |
| | | B to A | | 15.1 | | 10.1 | | 9.6 | | 8.6 | | 8.3 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 17.5 | | 14.5 | | 8.4 | | 6.5 | | 5.4 | ns |
| | | B to A | | 13.5 | | 9.6 | | 8.4 | | 7.7 | | 6.8 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 9.0 | | 9.0 | | 9.0 | | 9.0 | | 9.0 | ns |
| | | DIR to B | | 24.8 | | 23.8 | | 12.3 | | 10.1 | | 9.1 | ns |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 6.8 | | 6.8 | | 6.8 | | 6.8 | | 6.8 | ns |
| | | DIR to B | | 16.1 | | 14.6 | | 10.1 | | 9.6 | | 8.5 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 30.5 | | 24.5 | | 18.9 | | 18.1 | | 13.9 | ns |
| | | DIR to B | | 25.8 | | 23.7 | | 15.5 | | 13.1 | | 11.5 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 37.5 | | 32.5 | | 20.1 | | 17.8 | | 14.3 | ns |
| | | DIR to B | | 26.1 | | 23.0 | | 17.0 | | 14.8 | | 13.8 | ns |
| $V_{CC(A)}$=3.0V to 3.6V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 18.9 | | 17.0 | | 8.7 | | 6.2 | | 4.9 | ns |
| | | B to A | | 12.9 | | 8.0 | | 7.0 | | 6.2 | | 6.0 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 17.1 | | 13.8 | | 7.7 | | 5.5 | | 4.8 | ns |
| | | B to A | | 12.1 | | 7.9 | | 6.2 | | 5.5 | | 5.0 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 8.0 | | 8.0 | | 8.0 | | 8.0 | | 8.0 | ns |
| | | DIR to B | | 19.9 | | 18.3 | | 11.4 | | 9.6 | | 7.5 | ns |

## Electrical Characteristics (Cont.)

### AC Characteristics 2

Tamb=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.

| Parameter | Symbol | Conditions | VCC(B) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.5V±0.1V | | 1.8V±0.15V | | 2.5V±0.2V | | 3.3V±0.3V | | 5.0V±0.5V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 6.4 | | 6.4 | | 6.4 | | 6.4 | | 6.4 | ns |
| | | DIR to B | | 15.2 | | 14.0 | | 8.8 | | 8.1 | | 7.5 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 27.5 | | 21.3 | | 15.2 | | 13.9 | | 11.0 | ns |
| | | DIR to B | | 24.8 | | 22.8 | | 14.6 | | 12.0 | | 10.8 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 31.3 | | 25.6 | | 16.8 | | 14.6 | | 11.6 | ns |
| | | DIR to B | | 25.0 | | 21.7 | | 15.5 | | 13.3 | | 12.2 | ns |
| $V_{CC(A)}$=4.5V to 5.5V | | | | | | | | | | | | | |
| LOW to HIGH propagation delay | $t_{PLH}$ | A to B | | 18.1 | | 16.5 | | 8.5 | | 6.2 | | 4.3 | ns |
| | | B to A | | 11.4 | | 7.3 | | 5.5 | | 5.0 | | 4.3 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | A to B | | 16.5 | | 13.3 | | 6.9 | | 5.0 | | 4.0 | ns |
| | | B to A | | 11.4 | | 7.1 | | 5.1 | | 4.4 | | 4.0 | ns |
| HIGH to OFF state propagation delay | $t_{PHZ}$ | DIR to A | | 6.0 | | 6.0 | | 6.0 | | 6.0 | | 6.0 | ns |
| | | DIR to B | | 18.6 | | 17.5 | | 10.5 | | 8.8 | | 7.2 | ns |
| LOW to OFF state propagation delay | $t_{PLZ}$ | DIR to A | | 5.8 | | 5.8 | | 5.8 | | 5.8 | | 5.8 | ns |
| | | DIR to B | | 14.3 | | 13.0 | | 8.2 | | 7.8 | | 7.2 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | DIR to A | | 25.8 | | 20.6 | | 13.2 | | 12.0 | | 9.1 | ns |
| | | DIR to B | | 22.0 | | 20.5 | | 12.1 | | 10.0 | | 8.1 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | DIR to A | | 30.5 | | 25.6 | | 15.5 | | 12.8 | | 10.2 | ns |
| | | DIR to B | | 22.5 | | 19.5 | | 12.4 | | 10.6 | | 9.8 | ns |

Note:
[1] $t_{PZH}$ and $t_{PZL}$ are calculated values using the formula shown in Section 9.4.

## Testing Circuit

### AC Testing Circuit

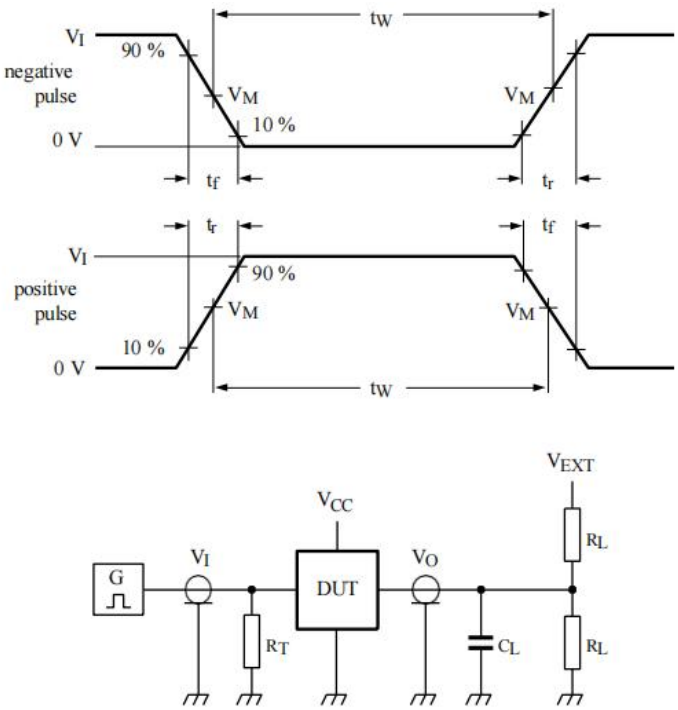



Figure 3. Test circuit for measuring switching times

$R_L$=Load resistance.
$C_L$=Load capacitance including jig and probe capacitance.
$R_T$=Termination resistance.
$V_{EXT}$=External voltage for measuring switching times.

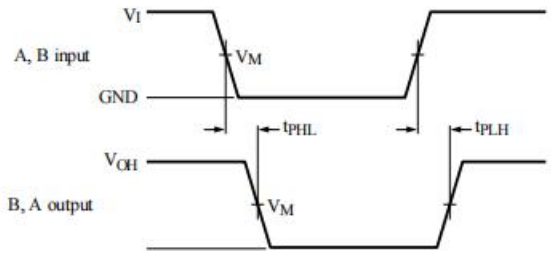
### Test Data

| Supply Voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | $V_I$[1] | Δt/ΔV[2] | $C_L$ | $R_L$ | tPLH, tPHL | tPZH, tPHZ | tPZL, tPLZ[3] |
| 1.2V to 5.5V | $V_{CCI}$ | ≤1.0ns/V | 15pF | 2kΩ | open | GND | $2V_{CCO}$ |

Note:
[1]$V_{CCI}$ is the supply voltage associated with the data input port.
[2]dV/dt≥1.0V/ns.
[3]$V_{CCO}$ is the supply voltage associated with the output port.

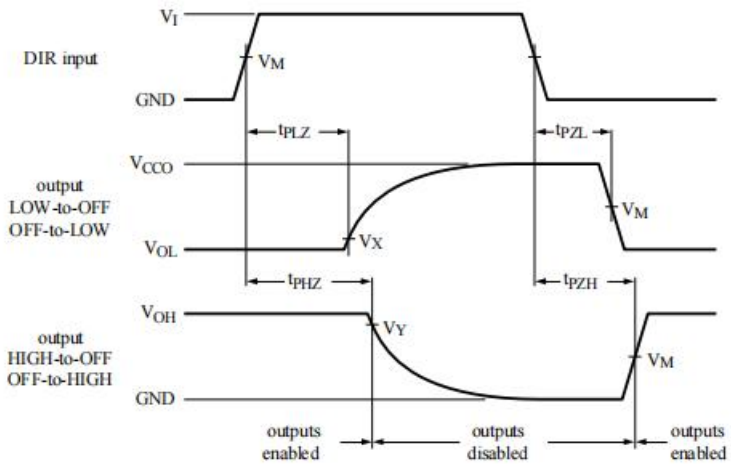
## Testing Circuit (Cont.)

### AC Testing Waveforms




$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Figure 4. The data input (A, B) to output (B, A) propagation delay times




VOL and VOH are typical output voltage levels that occur with the output load.

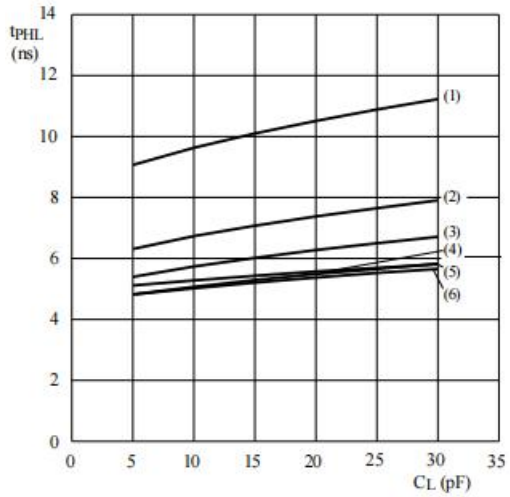
Figure 5. Enable and disable times

### Test Data

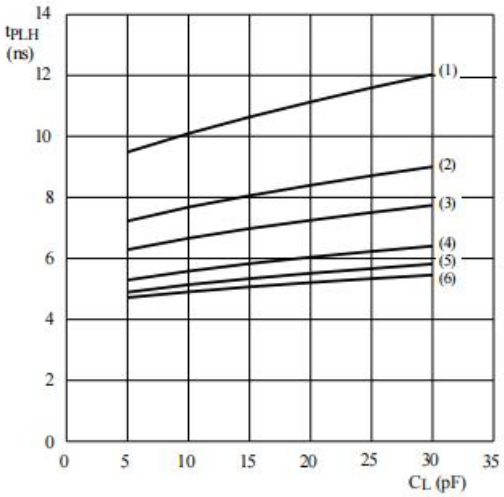
| Supply Voltage | Input[1] | Output[2] | | |
|---|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.2V to 1.6V | $0.5V_{CCI}$ | $0.5V_{CCI}$ | $V_{OL}$+0.1V | $V_{OH}$-0.1V |
| 1.65V to 2.7V | $0.5V_{CCI}$ | $0.5V_{CCI}$ | $V_{OL}$+0.15V | $V_{OH}$-0.15V |
| 3.0V to 5.5V | $0.5V_{CCI}$ | $0.5V_{CCI}$ | $V_{OL}$+0.3V | $V_{OH}$-0.3V |

Note:
[1]$V_{CCI}$ is the supply voltage associated with the data input port.
[2]$V_{CCO}$ is the supply voltage associated with the output port.

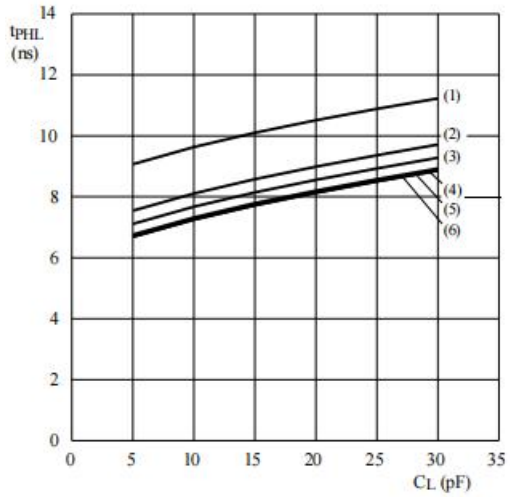
## Characteristic Curve



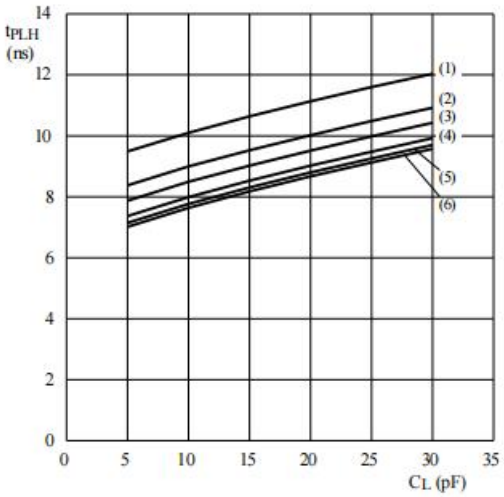

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)




c. HIGH to LOW propagation delay (B to A)

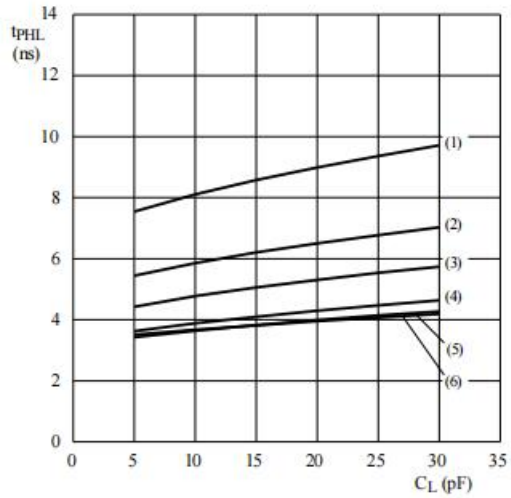



d. LOW to HIGH propagation delay (B to A)

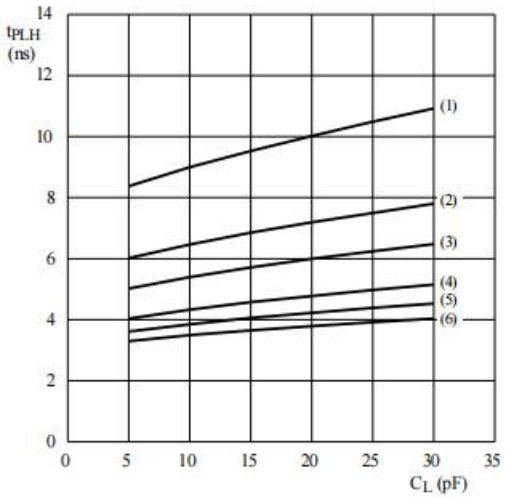
(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

Figure 6. Typical propagation delay vs load capacitance; Tamb = 25 °C; $V_{CC(A)}$ = 1.2 V

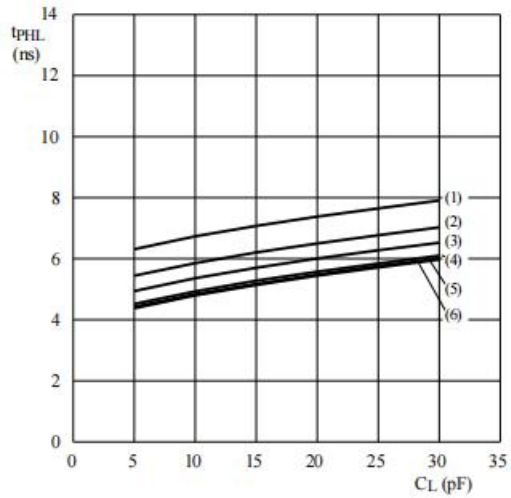
## Characteristic Curve (Cont.)



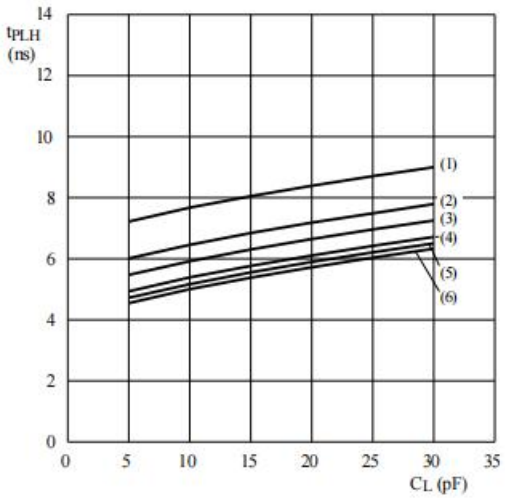

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)




c. HIGH to LOW propagation delay (B to A)

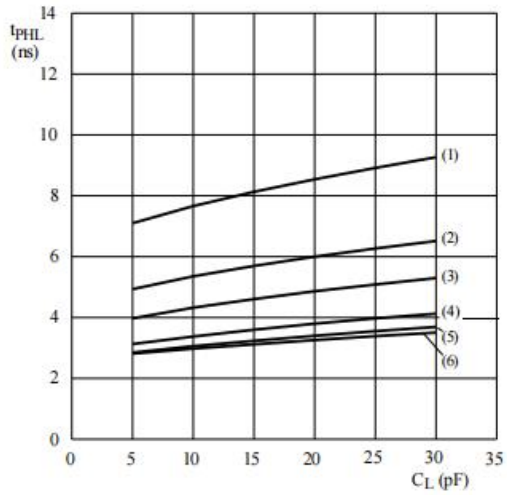



d. LOW to HIGH propagation delay (B to A)

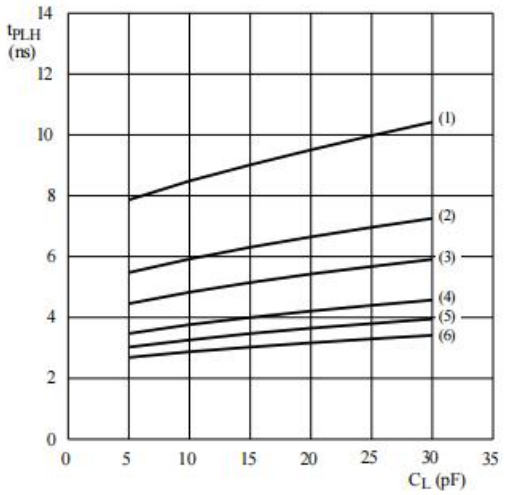
(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

Figure 7. Typical propagation delay vs load capacitance; Tamb = 25 °C; $V_{CC(A)}$ = 1.5 V

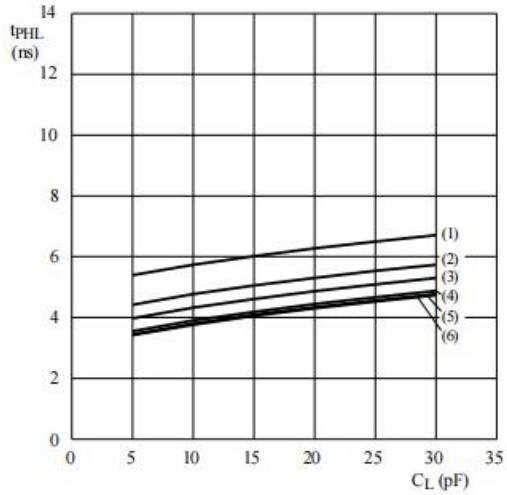
## Characteristic Curve (Cont.)



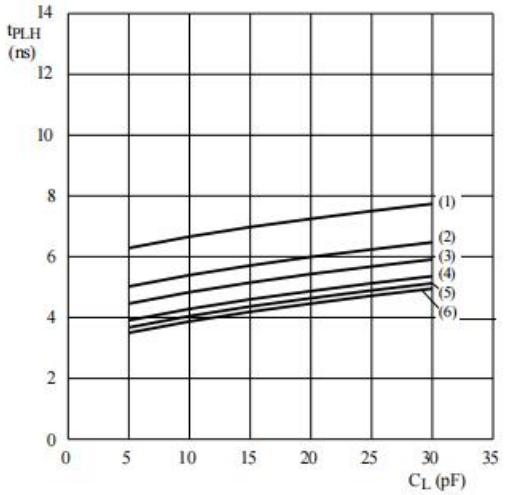

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)




c. HIGH to LOW propagation delay (B to A)

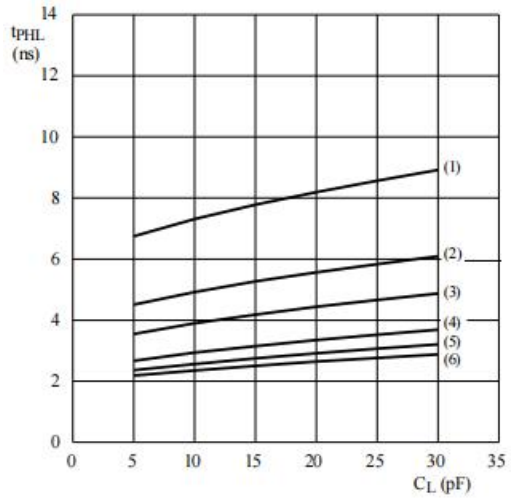



d. LOW to HIGH propagation delay (B to A)

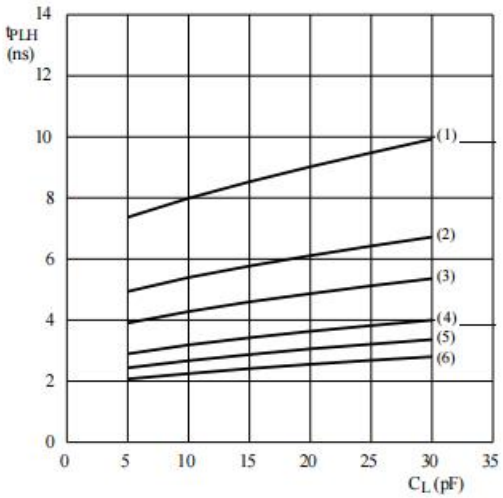
(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

Figure 8. Typical propagation delay vs load capacitance; Tamb = 25 °C; $V_{CC(A)}$ = 1.8 V

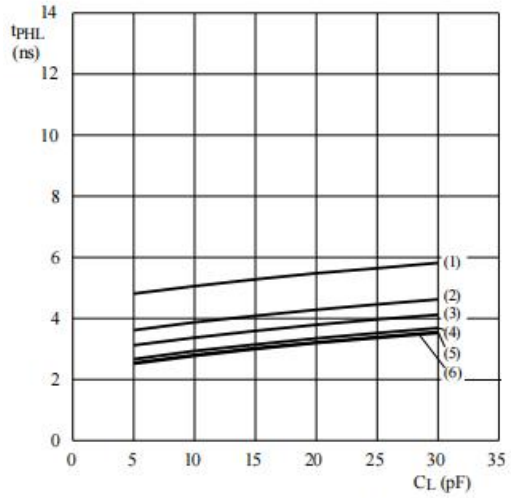
## Characteristic Curve (Cont.)



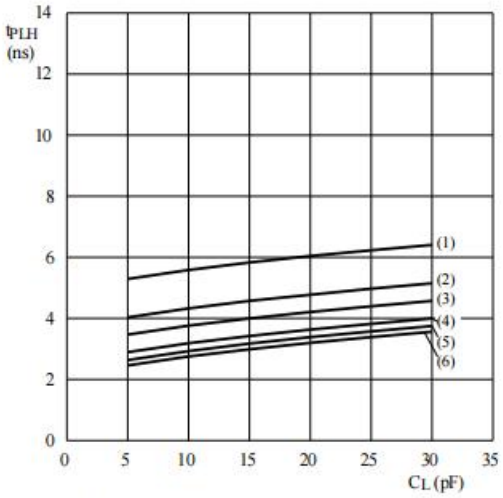

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)




c. HIGH to LOW propagation delay (B to A)

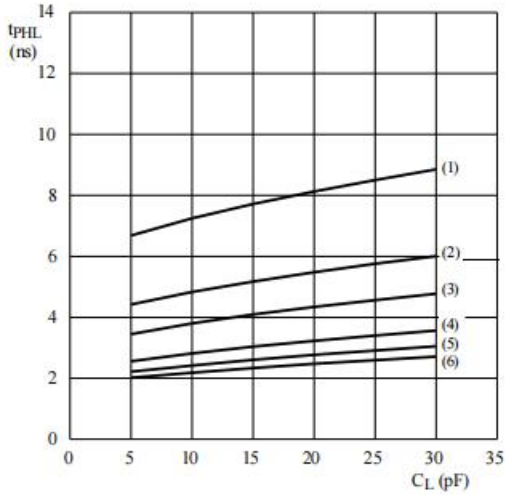



d. LOW to HIGH propagation delay (B to A)

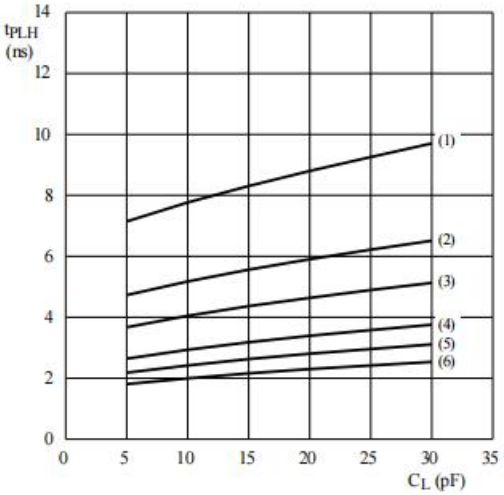
(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

Figure 9. Typical propagation delay vs load capacitance; Tamb = 25 °C; $V_{CC(A)}$ = 2.5 V

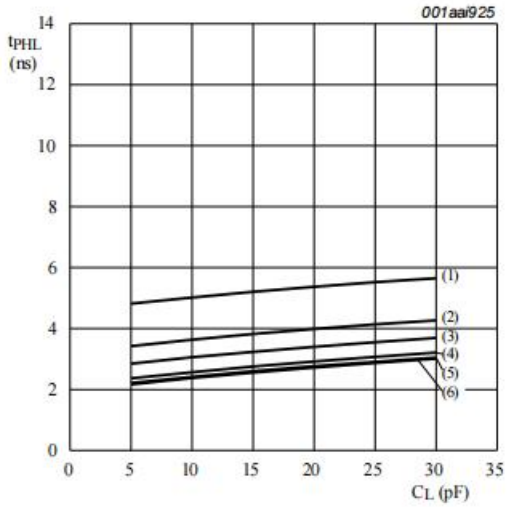
## Characteristic Curve (Cont.)



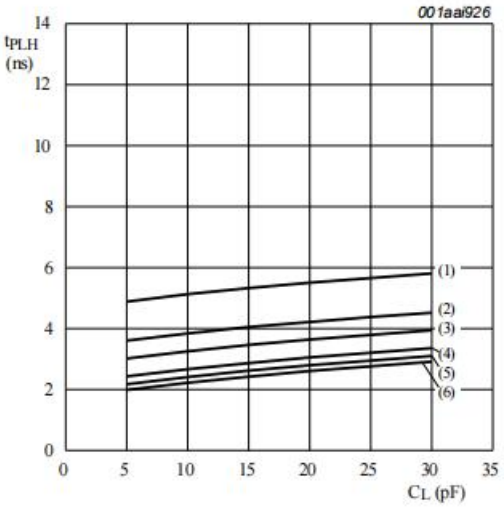

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)




c. HIGH to LOW propagation delay (B to A)

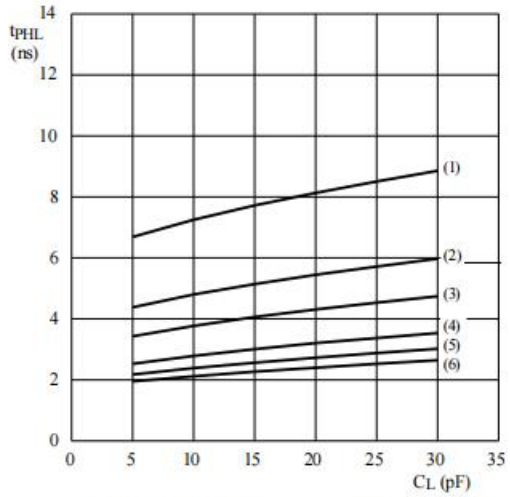



d. LOW to HIGH propagation delay (B to A)

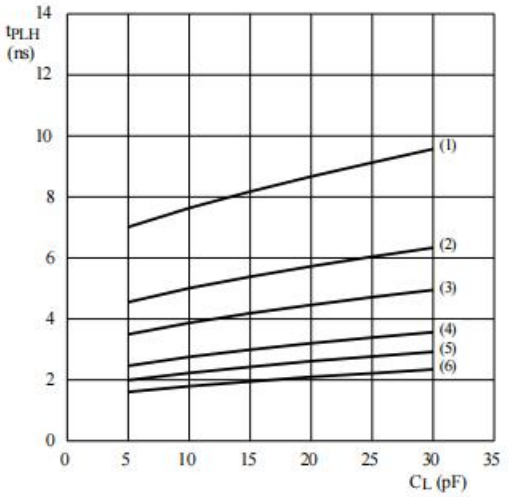
(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

Figure 10. Typical propagation delay vs load capacitance; Tamb = 25 °C; $V_{CC(A)}$ = 3.3 V

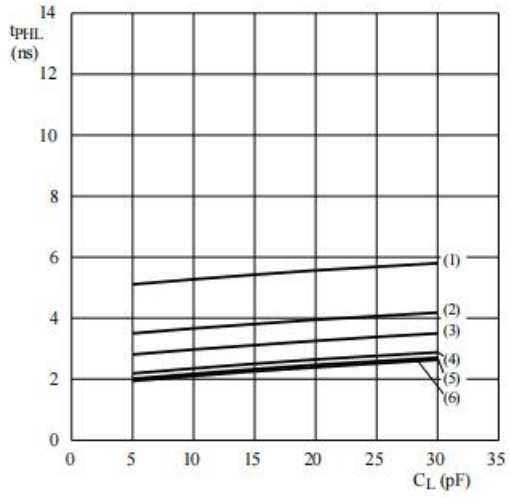
## Characteristic Curve (Cont.)



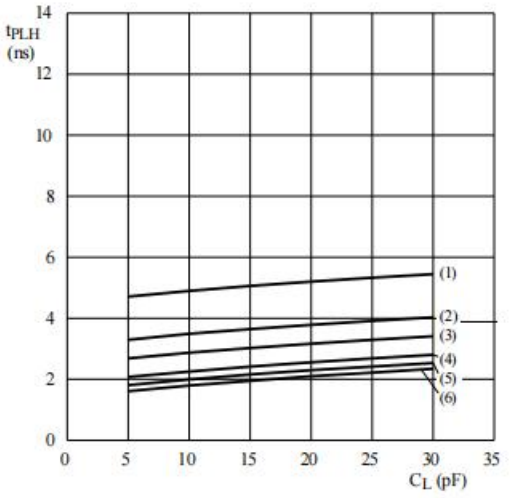

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)




c. HIGH to LOW propagation delay (B to A)




d. LOW to HIGH propagation delay (B to A)

(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

Figure 11. Typical propagation delay vs load capacitance; Tamb = 25 °C; $V_{CC(A)}$ = 5.0 V

## Typical Application Circuit And Application Note

### Unidirectional Logic Level-shifting Application

The circuit given in Figure 12 is an example of the LT74LVC1T45; LT74LVCH1T45 being used in a unidirectional logic level-shifting application.

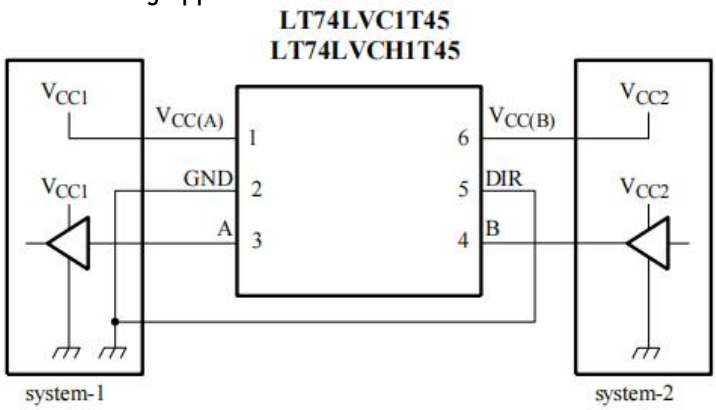


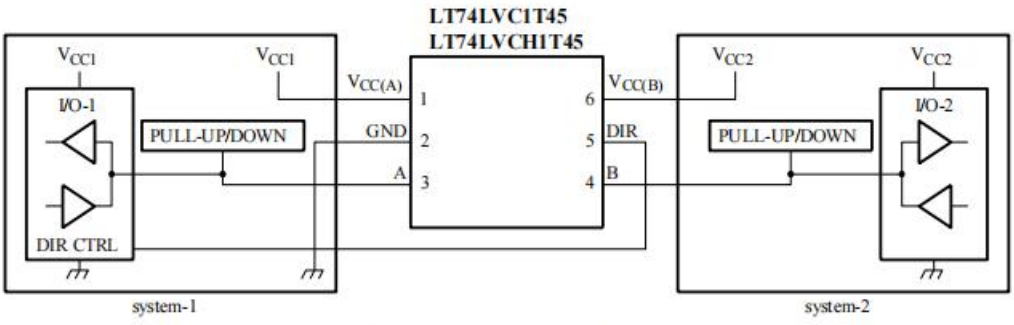

Figure 12. Unidirectional logic level-shifting application

| Pin | Name | Function | Description |
|---|---|---|---|
| 1 | $V_{CC(A)}$ | $V_{CC1}$ | Supply voltage of system-1 (1.2V to 5.5V). |
| 2 | GND | GND | Device GND. |
| 3 | A | OUT | Output level depends on $V_{CC1}$ voltage. |
| 4 | B | IN | Input threshold value depends on $V_{CC2}$ voltage. |
| 5 | DIR | DIR | The GND (LOW level) determines B port to A port direction. |
| 6 | $V_{CC(B)}$ | $V_{CC2}$ | Supply voltage of system-2 (1.2V to 5.5V) |

Table 1. Description of unidirectional logic level-shifting application

### Bidirectional Logic Level-shifting Application

Figure 13 shows the LT74LVC1T45; LT74LVCH1T45 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable pin, the system designer should take precautions to avoid bus contention between system-1 and system-2 when changing directions.




Pull-up or pull-down only needed for LT74LVC1T45.

Figure 13. Bidirectional logic level-shifting application

## Typical Application Circuit And Application Note (Cont.)

Table 2 gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

| State | DIR CTRL | I/O-1 | I/O-2 | Description |
|---|---|---|---|---|
| 1 | H | output | input | System-1 data to system-2. |
| 2 | H | Z | Z | system-2 is getting ready to send data to system-1.<br>I/O-1 and I/O-2 are disabled.<br>The bus-line state depends on bus hold. |
| 3 | L | Z | Z | DIR bit is set LOW.<br>I/O-1 and I/O-2 still are disabled.<br>The bus-line state depends on bus hold. |
| 4 | L | input | output | System-2 data to system-1. |

Table 2. Description of bidirectional logic level-shifting application

Note:
H=HIGH voltage level;
L=LOW voltage level;
Z=high-impedance OFF-state.

## Power-up Considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

| $V_{CC(A)}$ | $V_{CC(B)}$ | | | | | Unit |
|---|---|---|---|---|---|---|
| | 0V | 1.8V | 2.5V | 3.3V | 5.0V | |
| 0V | 0 | <1 | <1 | <1 | <1 | μA |
| 1.8V | <1 | <2 | <2 | <2 | 2 | μA |
| 2.5V | <1 | <2 | <2 | <2 | <2 | μA |
| 3.3V | <1 | <2 | <2 | <2 | <2 | μA |
| 5.0V | <1 | 2 | <2 | <2 | <2 | μA |

Table 3. Typical total supply current ($I_{CC(A)}$+$I_{CC(B)}$)

## Enable Times

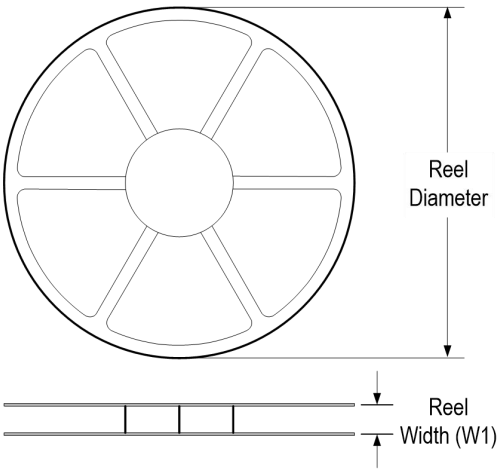
Calculate the enable times for the LT74LVC1T45; LT74LVCH1T45 using the following formulas:

$t_{PZH}$(DIR to A)=$t_{PLZ}$(DIR to B)+$t_{PLH}$(B to A)
$t_{PZL}$(DIR to A)=$t_{PHZ}$(DIR to B)+$t_{PHL}$(B to A)
$t_{PZH}$(DIR to B)=$t_{PLZ}$(DIR to A)+$t_{PLH}$(A to B)
$t_{PZL}$(DIR to B)=$t_{PHZ}$(DIR to A)+$t_{PHL}$(A to B)

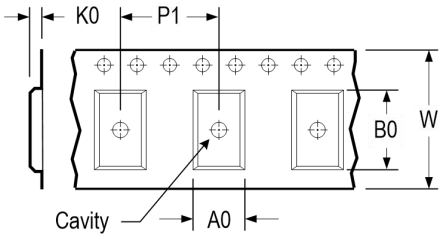
In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the LT74LVC1T45; LT74LVCH1T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay

## Tape and Reel Information

### REEL DIMENSIONS

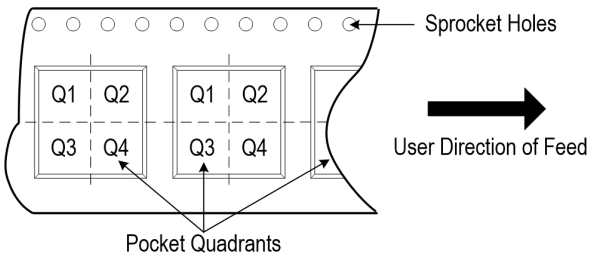



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

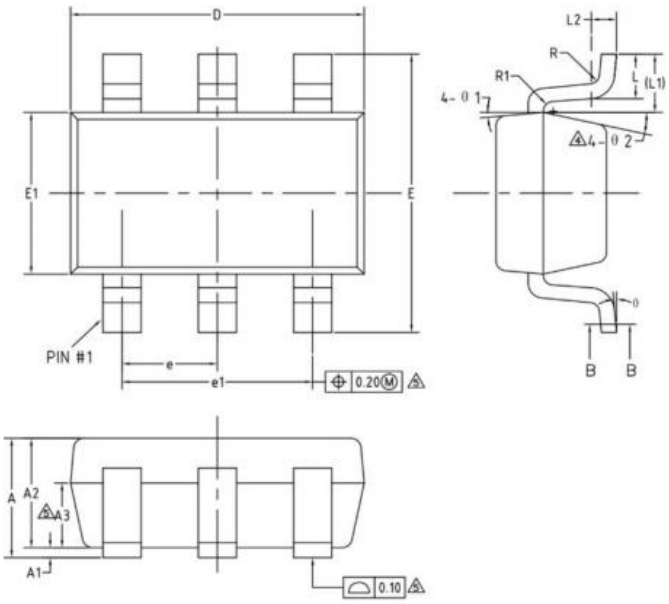



* All dimensions are nominal

| Device | Package Type | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin 1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LT74LVC1T45XT6/R6 | SOT23 | 6 | 3 000 | 178 | 9.5 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LT74LVC1T45XC6/R6 | SC70 | 6 | 3 000 | 178 | 10.0 | 4.0 | 3.5 | 1.5 | 4.0 | 8.0 | Q3 |
| LT74LVCH1T45XT6/R6 | SOT23 | 6 | 3 000 | 178 | 9.5 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LT74LVCH1T45XC6/R6 | SC70 | 6 | 3 000 | 178 | 10.0 | 4.0 | 3.5 | 1.5 | 4.0 | 8.0 | Q3 |

## Package Dimension

SOT23-6L

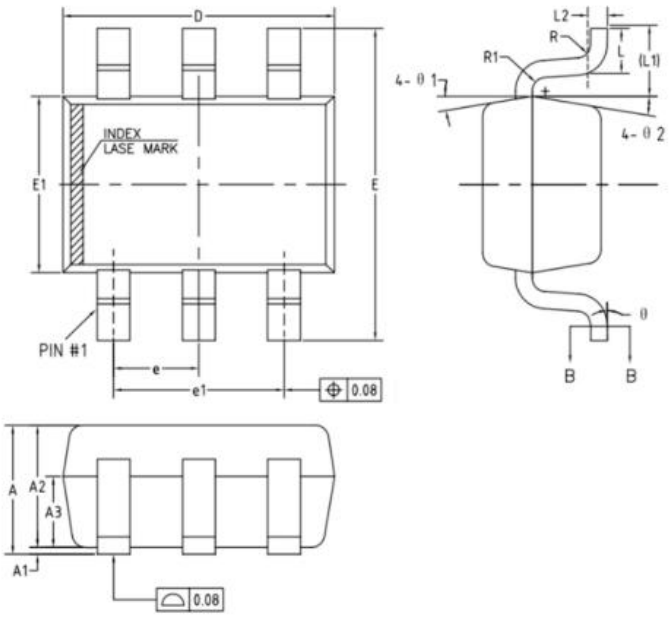



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|
| | A | – | – | 1.25 |
| | A1 | 0 | – | 0.15 |
| | A2 | 1.00 | 1.10 | 1.20 |
| | A3 | 0.60 | 0.65 | 0.70 |
| | b | 0.36 | – | 0.50 |
| | b1 | 0.36 | 0.38 | 0.45 |
| | c | 0.14 | – | 0.20 |
| | c1 | 0.14 | 0.15 | 0.16 |
| | D | 2.826 | 2.926 | 3.026 |
| | E | 2.60 | 2.80 | 3.00 |
| | E1 | 1.526 | 1.626 | 1.726 |
| 4 | e | 0.90 | 0.95 | 1.00 |
| 4 | e1 | 1.80 | 1.90 | 2.00 |
| | L | 0.35 | 0.45 | 0.60 |
| | L1 | 0.59REF | | |
| | L2 | 0.25BSC | | |
| 3 | R | 0.10 | – | – |
| 3 | R1 | 0.10 | – | 0.20 |
| | θ | 0° | – | 8° |
| | θ1 | 3° | 5° | 7° |
| 4 | θ2 | 6° | – | 14° |

## Package Dimension (Cont.)

SC70-6L




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.85 | – | 1.05 |
| A1 | 0 | – | 0.10 |
| A2 | 0.80 | 0.90 | 1.00 |
| A3 | 0.47 | 0.52 | 0.57 |
| 2 b | 0.22 | – | 0.29 |
| b1 | 0.22 | 0.25 | 0.28 |
| 3 2 c | 0.115 | – | 0.15 |
| 3 c1 | 0.115 | 0.13 | 0.14 |
| D | 2.02 | 2.07 | 2.12 |
| E | 2.20 | 2.30 | 2.40 |
| E1 | 1.25 | 1.30 | 1.35 |
| e | 0.65BSC | | |
| e1 | 1.30BSC | | |
| L | 0.28 | 0.33 | 0.38 |
| L1 | 0.50REF | | |
| L2 | 0.15BSC | | |
| R | 0.10 | – | – |
| R1 | 0.10 | – | 0.25 |
| θ | 0° | – | 8° |
| θ 1 | 6° | 9° | 12° |
| θ 2 | 6° | 9° | 12° |

## Important Notice

Linearin is a global fabless semiconductor company specializing in advanced high-performance high-quality analog/mixed-signal IC products and sensor solutions. The company is devoted to the innovation of high performance, analog-intensive sensor front-end products and modular sensor solutions, applied in multi-market of medical & wearable devices, smart home, sensing of IoT, intelligent industrial & smart factory (industrial 4.0), and automotives. Linearin's product families include widely-used standard catalog products, solution-based application specific standard products (ASSPs) and sensor modules that help customers achieve faster time-to-market products. Go to http://www.linearin.com for a complete list of Linearin product families.

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