

General Description

The LTP842Q are ultra-low quiescent current, low dropout linear regulators (LDOs) with a wide input voltage range of 2.75V to 40V. The series provides 3.3V, 5V and 15V fixed outputs or 0.6V to 24V adjustable output and delivers up to 200mA output current. The shutdown current of LTP842Q is less than 1 μ A, while the quiescent current under no-load condition is less than 7.5 μ A.

LTP842Q provides a power good indicator with programmable delay to directly drive the reset pin of a microprocessor (MCU). Moreover, there are options of highly accurate fixed output of 3.3V or 5V. LTP842Q features over-current protection and over-temperature shutdown with auto restart. The product family is available in thermally enhanced SOT23-5L, SOT23-5R, EMSOP-8L and ESOP-8L packages.

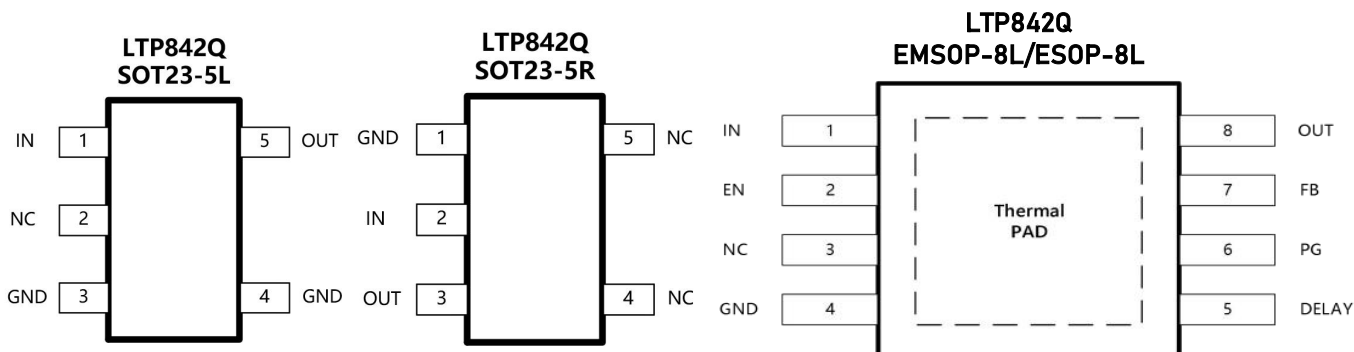
Features and Benefits

- Ultra-Low I_Q < 7.5 μ A
- Wide Input Voltage Range: 2.75V to 40V
- $\pm 2\%$, 3.3V, 5V and 15V Fixed Outputs and 0.6V to 24V Adjustable Output
- Up to 200mA Output Current
- Shutdown Current < 1 μ A
- PG Indicator with Adjustable Delay for MCU Applications
- High PSRR: 82dB at 100Hz
- Stable Closed-Loop Operation with only 1 μ F Low-ESR Ceramic Output Capacitor
- Low Dropout: 210mV at 200mA
- Up to 40V High Voltage EN Pin with Logic Threshold
- Over-Current Protection
- Over-Temperature Shutdown and Auto Restart
- Internal Soft Start
- -40°C to 150°C Junction Temperature
- Thermally Enhanced SOT23-5L, SOT23-5R, EMSOP-8L and ESOP-8L Packages
- Thermal Shutdown Protection
- Automotive AEC-Q100 Grade 1 Compliance

Applications

- Industrial Power Supplies
- Battery Powered Systems
- Automotive Power Supplies

Pin Description (Top View)



Pin Function

Package/NC			Symbol	Function
SOT23-5L	SOT23-5R	EMSOP-8L/ ESOP-8L		
1	2	1	IN	Input Pin, place a ceramic capacitor of at least 1 μ F between IN and GND.
/	/	2	EN	Enable pin, connect to a logic control signal or IN directly.
2	4/5	3	NC	No connect.
3/4	1	4	GND	Connect to GND.
/	/	5	DELAY	Power good delay pin, place a ceramic capacitor between Delay and GND.
/	/	6	PG	Power good pin, open drain, connect a pull-up resistor between PG and an external supply or to OUT pin, if not used, keep floating.
/	/	7	FB	Feedback Pin, connect to the center leg of the voltage divider between OUT and GND. This pin has no internal connection for fixed output versions.
5	3	8	OUT	Output pin, place a ceramic capacitor of at 1 μ F between OUT and GND.

Ordering Information

Package Type	Part Number	Quantity	Mark Code
SOT23-5L	LTP842-33QT5/R6	Tape and Reel, 3 000	GQC33
SOT23-5R	LTP842-33RQT5/R6	Tape and Reel, 3 000	GQCR3
EMSOP-8L	LTP842-AEQV8/R6	Tape and Reel, 3 000	Q842
ESOP-8L	LTP842-AEQS8/R8	Tape and Reel, 4 000	Q842

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage	V _{IN}	-0.3 to 45	V
Output Voltage	V _{OUT}	-0.3 to V _{IN}	V
Enable Voltage	V _{EN}	-0.3 to V _{IN}	V
Delay Voltage	V _{Delay}	-0.3 to 5	V
PG Voltage	V _{PG}	0.3 to 40	V
Junction Temperature	T _J	-40 to 150	°C
Storage Temperature	T _{STG}	-55 to 150	°C

ESD Ratings

Parameter	Level	Unit
Human body model (HBM), per AEC-Q100-002	2 000	V
Charged device model (CDM), per AEC-Q100-011	750	

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V _{IN}	Input Voltage	-0.3 to 40	V
V _{EN}	Enable Voltage	-0.3 to V _{IN}	V
I _{OUT}	Output Current	0 to 400	mA
V _{PG}	PG Voltage	0.3 to 40	V
V _{Delay}	Delay Voltage	0 to 4	V
T _J	Junction Temperature	-40 to 150	°C

Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40°C to 150°C . Typical values are measured at 25°C and represent the most likely norm. The default conditions apply: $V_{\text{IN}} = 13.5\text{V}$.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN, VOUT(IN, OUT, GND, PINS)						
Input Voltage Operation Range	VIN		2.7		40	V
Operating Output Voltage Range for Adjustable Output	VOUT		0.6		24	V
Input Shutdown Current	IQ-SH	VEN = 0mV, VIN = 13.5V		0.8		μA
Input Quiescent Current	IQ-NL	VEN = 5V, VIN = 13.5V, IOUT = 0A		11	15	μA
Input Quiescent Current with PG Function	IQ-NL	VEN = 5V, VIN = 13.5V, IOUT = 0A		11	15	μA
REGULATION(OUT,FB PINS)						
Regulated Feedback Voltage	VFB	VFB=VOUT, 28V > VIN > 4.3V, IOUTMAX > IOUT > 1mA VFB=VOUT, 40 > VIN > 28V, 75%*IOUTMAX > IOUT > 1mA		0.6		V
Feedback Input Leakage Current	IFB	VFB=0.6V	-0.1	0	0.1	μA
Output Voltage Accuracy	VOUT%	28V>VIN > VOUT+1V, IOUTMAX > IOUT > 1mA 40V>VIN>28V, 75%*IOUTMAX > IOUT > 1mA	-2		2	%
Line Regulation		40V > VIN > VOUT+1V, 75%*IOUTMAX > IOUT > 1mA		±0.1		%
Load Regulation		40V > VIN > VOUT+1V, 75%*IOUTMAX > IOUT > 1mA		±0.5		%
DROPOUT						
Drop Out Voltage	VDO-100mA	IOUT = 100mA, VIN= 0.9*VOUT, VOUT > =5V		130		mV
	VDO-200mA	IOUT = 200mA, VIN= 0.9*VOUT, VOUT > =5V		210		
	VDO-100mA-3.3V	IOUT = 100mA, VIN= 0.9*VOUT, VOUT=3.3V		150		
	VDO-200mA-3.3V	IOUT = 200mA, VIN= 0.9*VOUT, VOUT=3.3V		300		
OVER CURRENT PROTECTION						
Current Limit Threshold	ILIMIT-200mA			386	500	mA
POWER SUPPLY REJECTION RATIO(PSRR)						
PSRR@100Hz	GPSRR-100Hz	IOUT = 50mA,VOUT=3.3V or 5V		82		dB
ENABLE(EN PIN)						
EN Pin Voltage Range	VEN	IOUT = 100mA, VIN=0.9*VOUT, VOUT >=5V	-0.3		VIN	V
EN Enable Threshold Voltage	VEN-H	IOUT = 200mA, VIN=0.9*VOUT, VOUT >=5V	2			V

Electrical Characteristics (Cont.)

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40°C to 150°C . Typical values are measured at 25°C and represent the most likely norm. The default conditions apply: $V_{\text{IN}} = 13.5\text{V}$.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Disable Threshold Voltage	$V_{\text{EN-L}}$	$I_{\text{OUT}} = 100\text{mA}$, $V_{\text{IN}} = 0.9 \cdot V_{\text{OUT}}$, $V_{\text{OUT}} = 3.3\text{V}$			0.4	V
EN Leakage Current	$I_{\text{EN-H}}$	$I_{\text{OUT}} = 200\text{mA}$, $V_{\text{IN}} = 0.9 \cdot V_{\text{OUT}}$, $V_{\text{OUT}} = 3.3\text{V}$	0.5		2	μA

THERMAL SHUTDOWN

Thermal Shutdown Threshold				170		$^{\circ}\text{C}$
Thermal Shutdown Recovery Hysteresis				20		$^{\circ}\text{C}$

POWER GOOD(PG,DELAY PINS)

Power good Rising Threshold	$V_{\text{PG-RISE}}$	V_{FB} , Ramping Up	87	92.5	98	%
Power good Falling Threshold	$V_{\text{PG-FALL}}$	V_{FB} , Ramping Down	83.5	88	92.5	%
Power good Internal Pull-Down Resistor	$R_{\text{PG-DN}}$			330		Ω
Delay Capacitor Charge Current	$I_{\text{D-CHARGE}}$	$V_{\text{D}} = 1\text{V}$		2.01		μA
Delay Capacitor Discharge Current	$I_{\text{D-DISCHARGE}}$	$V_{\text{D}} = 1\text{V}$		12.5		mA
Delay Rising Threshold	$V_{\text{D-RISE}}$			0.75		V
Delay Falling Threshold	$V_{\text{D-FALL}}$			1.0		V

Typical Performance Characteristics

$C_{IN} = 1\mu F$, $C_{OUT} = 22\mu F$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

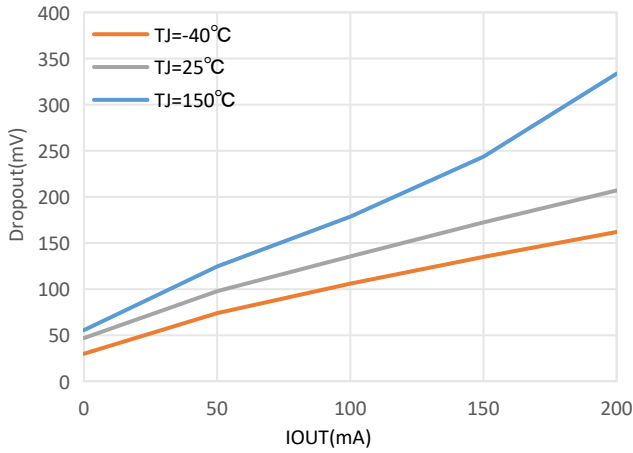


Figure 1. Dropout Voltage vs Output Current
($V_{OUT} = 5V$)

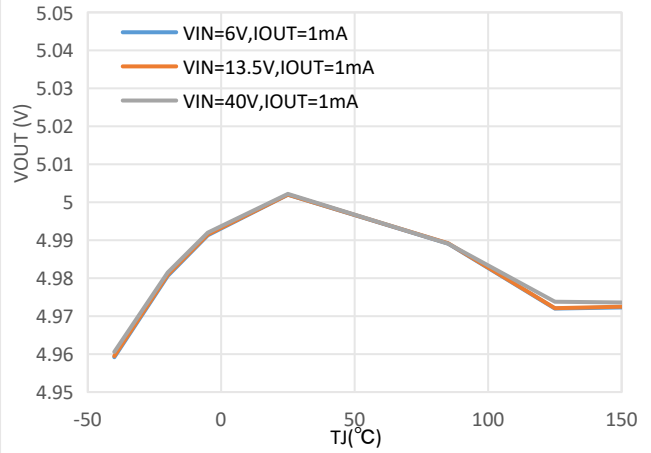


Figure 2. Output Voltage vs Junction Temperature
($V_{OUT} = 5V$)

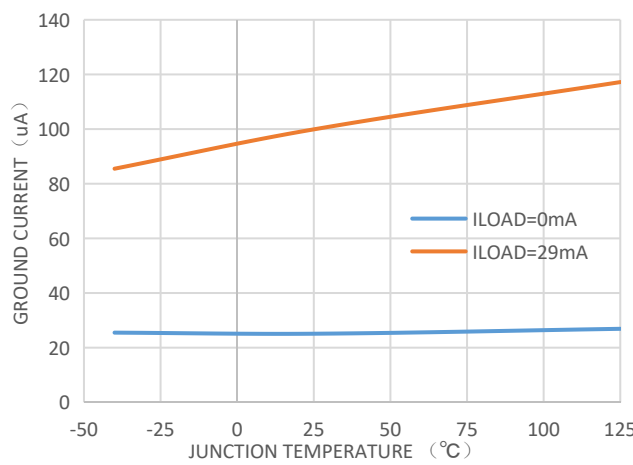


Figure 3. GND Current vs Junction Temperature
($V_{IN} = 13.5V$)

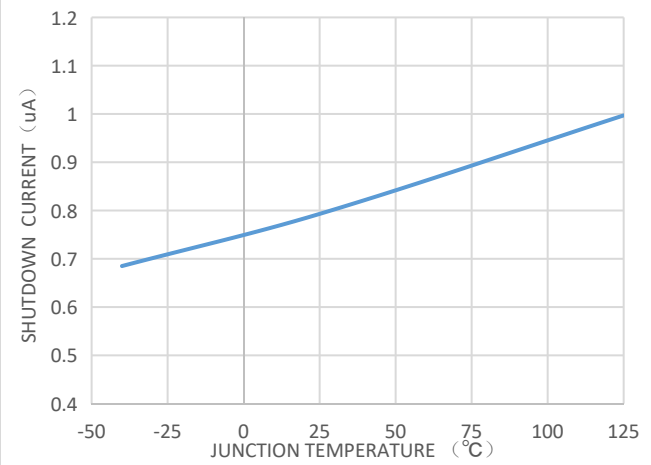


Figure 4. Shutdown Current vs Junction Temperature
($V_{IN} = 13.5V$)

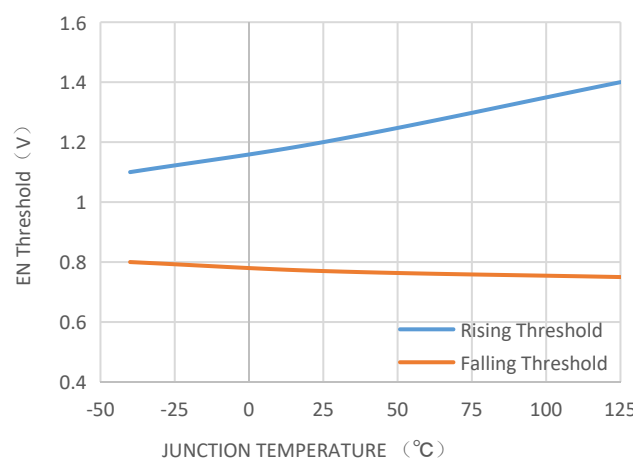


Figure 5. EN Threshold vs Junction Temperature
($V_{IN} = 13.5V$)

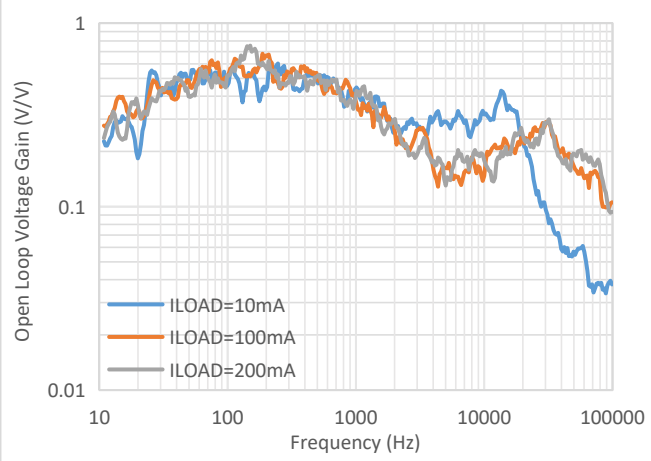


Figure 6. Open Loop Voltage Gain vs Frequency

Typical Performance Characteristics (Cont.)

$C_{IN} = 1\mu F$, $C_{OUT} = 22\mu F$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

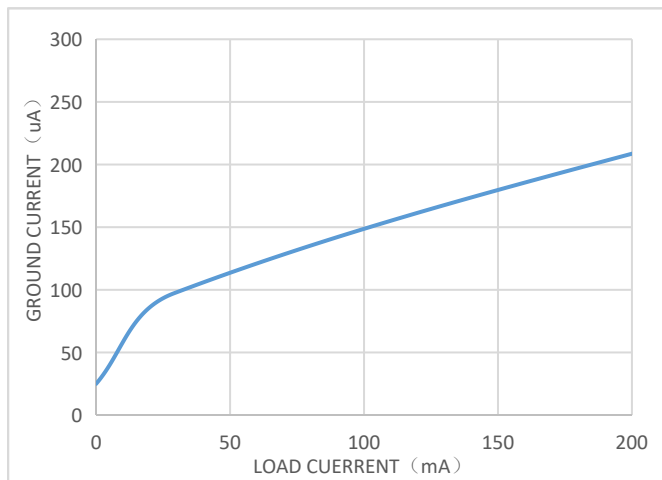


Figure 7. Ground Current vs Load Current
($V_{IN} = 6V$)

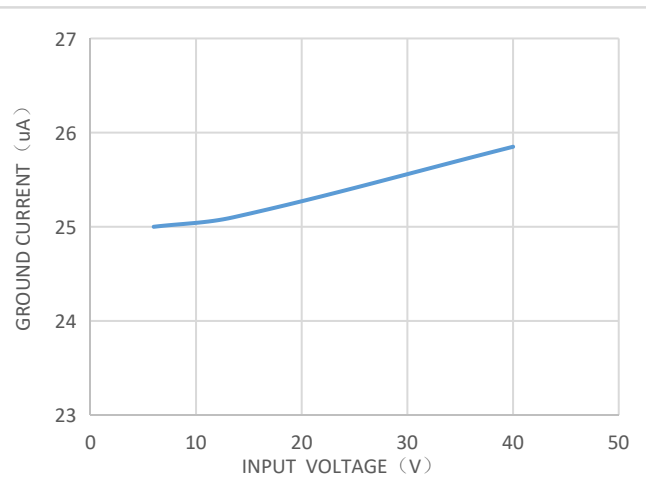


Figure 8. Ground Current vs V_{IN}
($I_{OUT} = 0mA$)

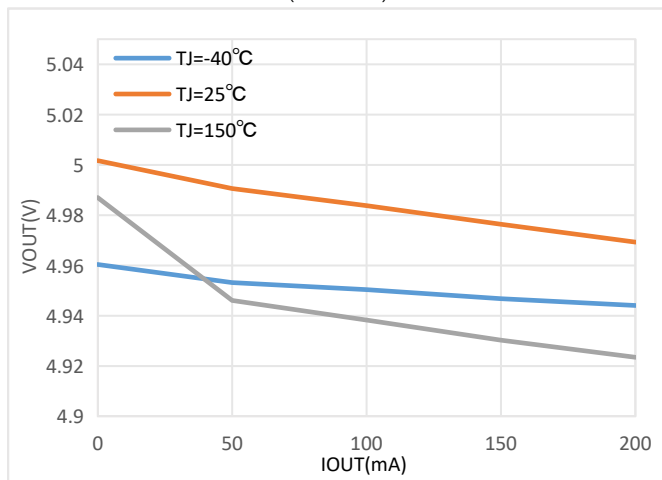


Figure 9. Load Regulation
($V_{IN} = 13.5V$)

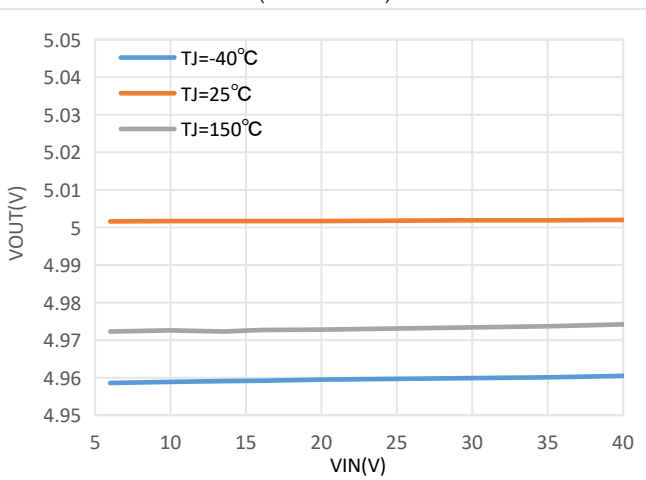


Figure 10. Line Regulation
($I_{OUT} = 1mA$)

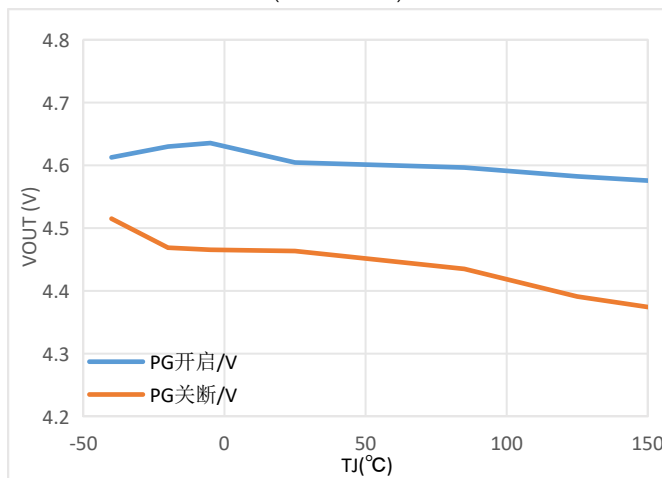


Figure 11. PG vs. Temperature

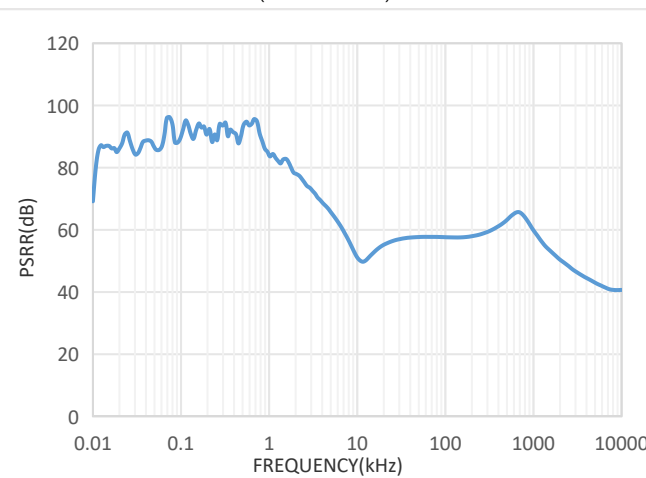


Figure 12. PSRR vs Frequency

Typical Performance Characteristics (Cont.)

$C_{IN} = 1\mu F$, $C_{OUT} = 22\mu F$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

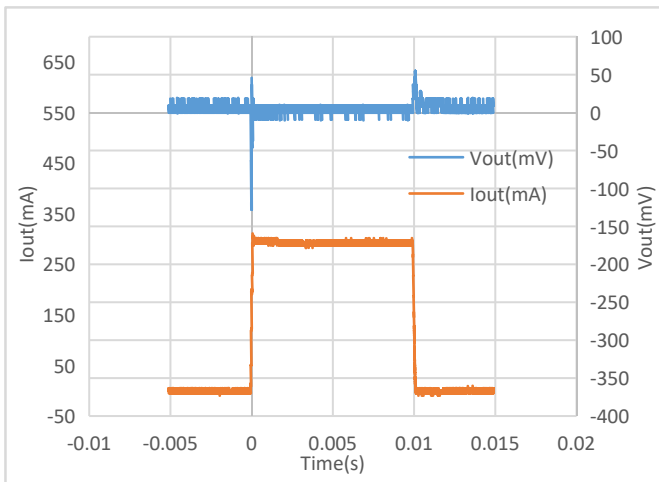


Figure 13. Load Transient ($V_{IN} = 12V$, $I_{OUT} = 200mA$)

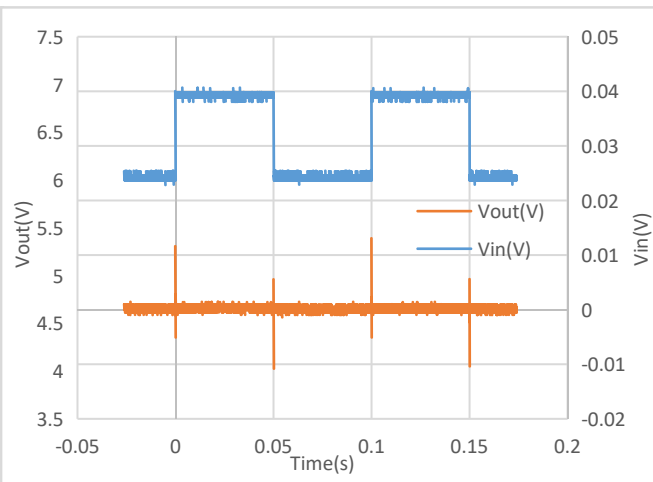


Figure 14. Line Transient ($V_{IN} = 6V-7V$, $I_{OUT} = 200mA$)

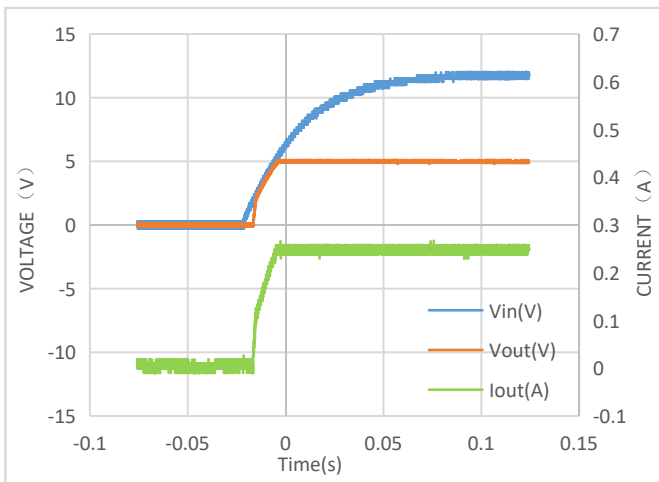


Figure 15. Start-Up through V_{IN}
($V_{IN} = 12V$, $I_{OUT} = 300mA$)

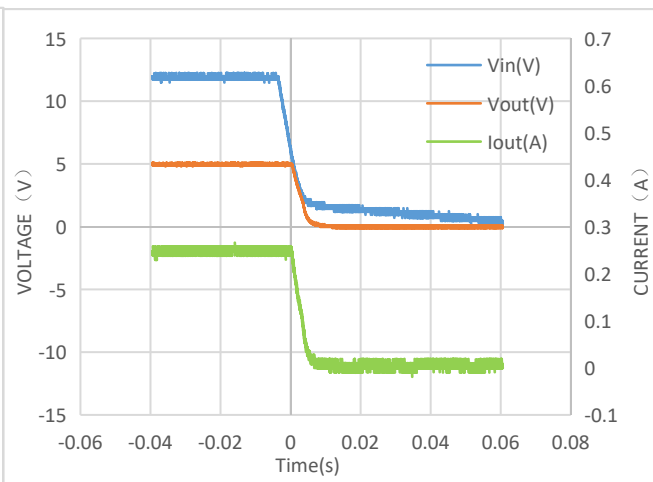


Figure 16. Shutdown through V_{IN}
($V_{IN} = 12V$, $I_{OUT} = 300mA$)

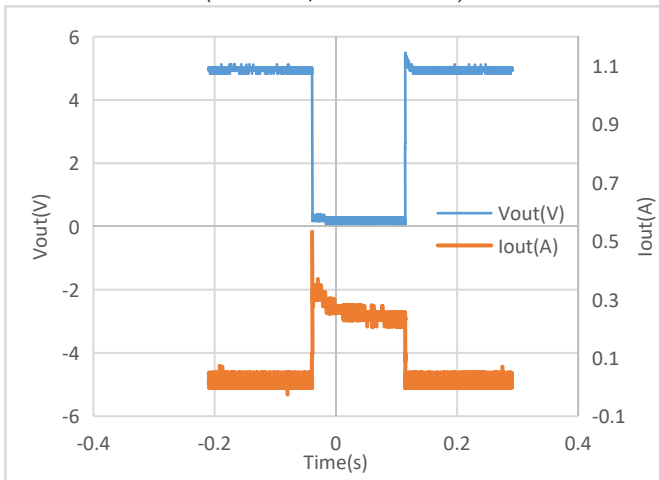


Figure 17. Short-Circuit Entry and Recovery

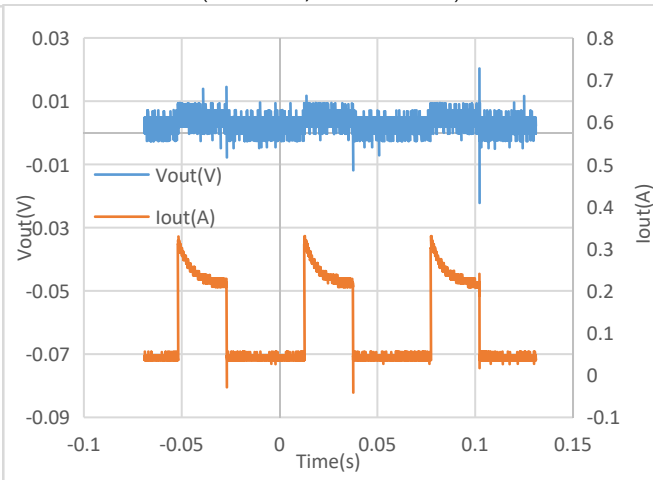
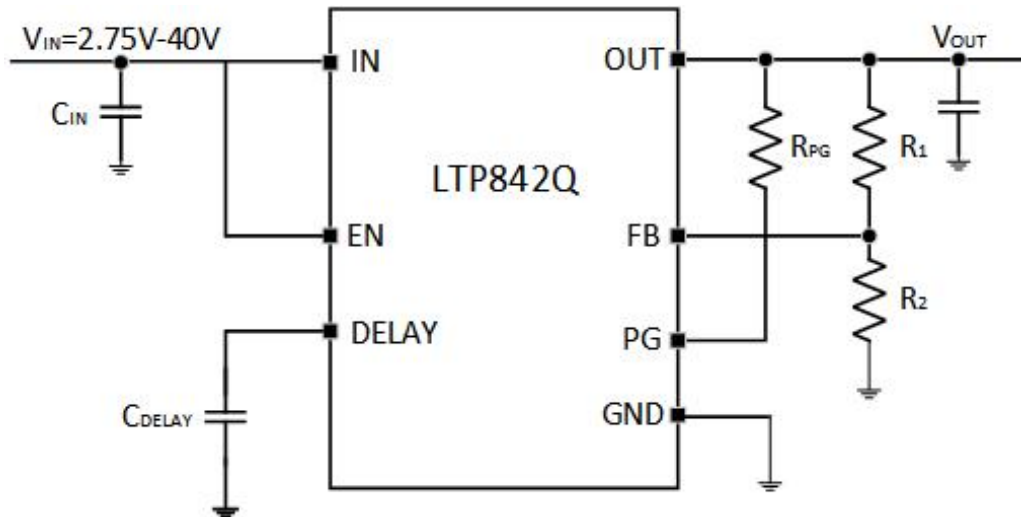


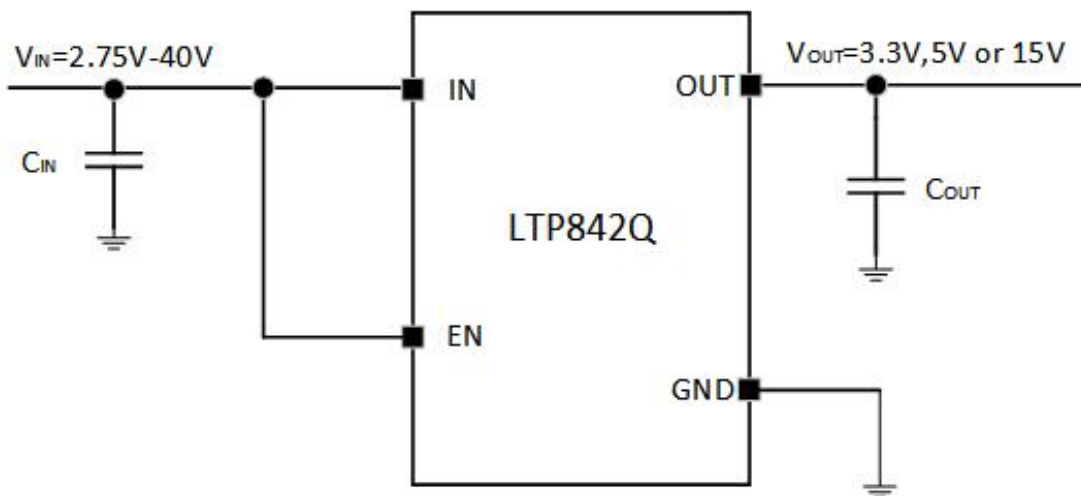
Figure 18. Short-Circuit Steady State ($V_{IN} = 12V$)

Application

Application Diagram with Full Features



Minimum Application Diagram



Application (Cont.)

Application Considerations

Input and Output Decoupling Capacitors

For control-loop stability, LTP842Q integrates internal compensation and only requires ceramic capacitors with minimum capacitance of 1 μF between VIN and GND and VOUT and GND, respectively. It is recommended that the capacitor is placed as close to the device pins as possible with minimum PCB trace length.

EN Pin

EN is the enable pin of the internal device supply and the output of the LDO. When the voltage on EN pin rises above the rising threshold VEN-H, the LDO output is allowed; and when the voltage on EN falls below the falling threshold VEN-L, the LDO output is disabled and the device goes into shutdown mode. Another way of using EN pin is connecting EN directly to the input voltage, the pin has the same maximum operating voltage of 40V as the LDO input.

OUT and FB Pins

To adjust the output voltage, connect a voltage divider between OUT and GND, and connect the center of the divider to FB pin. The steady state VFB is typically at 0.6V. The output voltage can be derived from:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$$

Fully utilize the low IQ capability of the product family, it is recommended to use resistors with tolerance better than 1% and with temperature coefficients less than 100ppm for the divider design. A typical selection of R2 is 100kΩ, R1 can then be calculated from:

$$R_1 = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R_2$$

When using the fixed V_{OUT} products, there is no external divider.

PG and DELAY Pins

The PG pin is connected to the open drain of an internal N-MOSFET. Externally, the PG pin needs to be pulled up to a voltage source by a resistor. The PG pin can directly drive the reset pin of a MCU. When EN is high and V_{OUT} rises above the power good threshold V_{PG-RISE}, the DELAY pin starts to output a current I_{D-Charge} to charge the external delay capacitor, when the voltage on the DELAY pin rises across V_{D-RISE}, PG is pulled up. The external delay capacitor is selected based on the desired MCU delay t_{Delay} and is calculated based on:

$$C_{Delay} = \frac{t_{Delay} \times I_{D-Charge}}{V_{D-Rise}}$$

Functional Description

Overview

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Functional Diagram

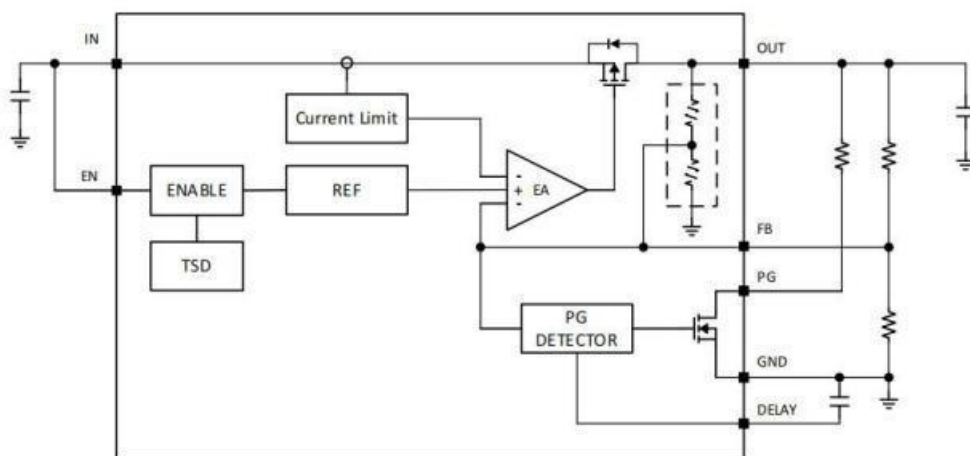
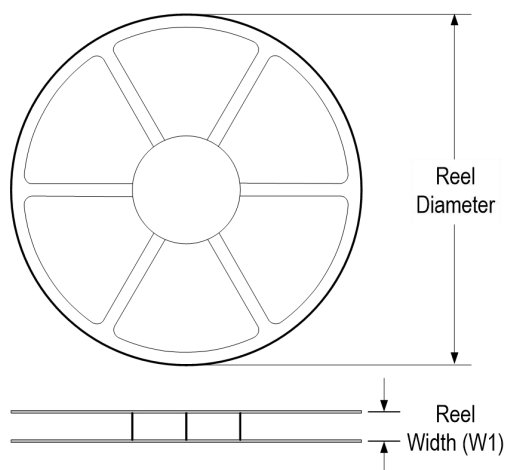


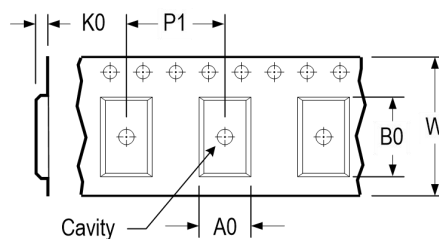
Figure 1: LTP842Q Functional Diagram (The fixed version is inside the dashed box)

Tape and Reel Information

REEL DIMENSIONS

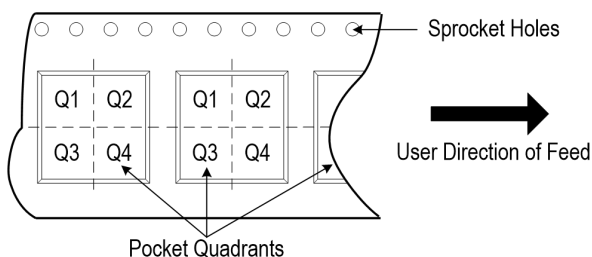


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

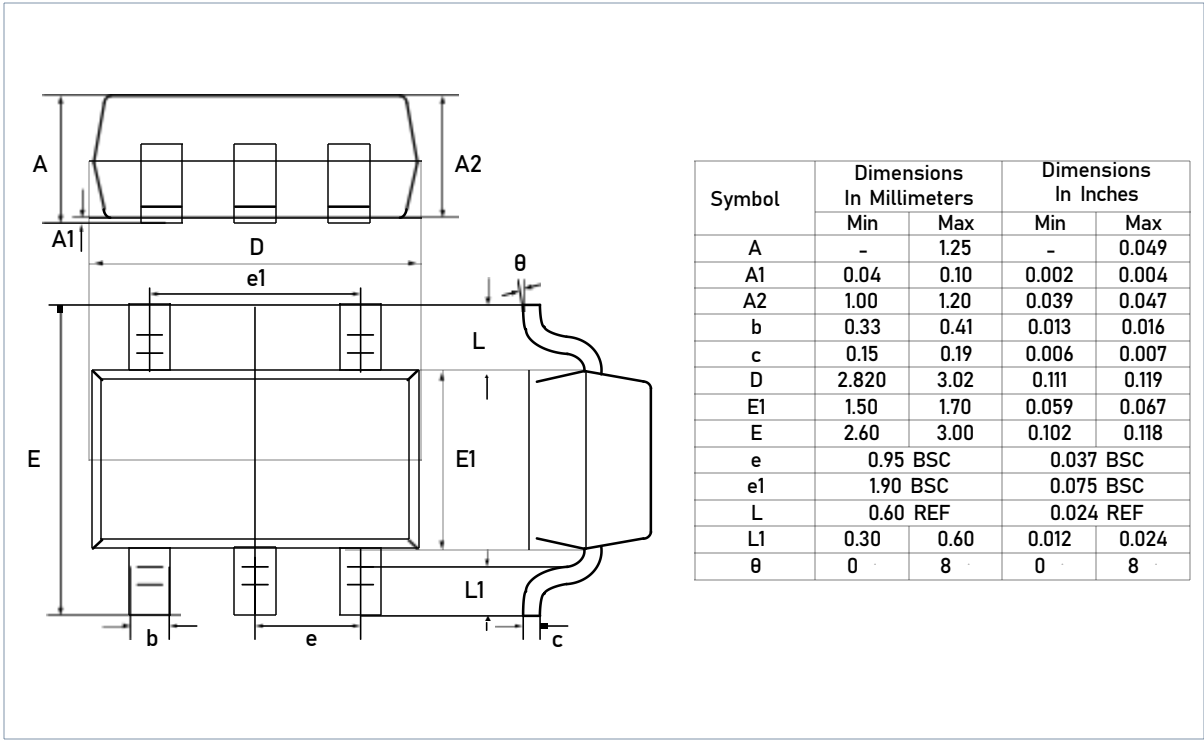


* All dimensions are nominal

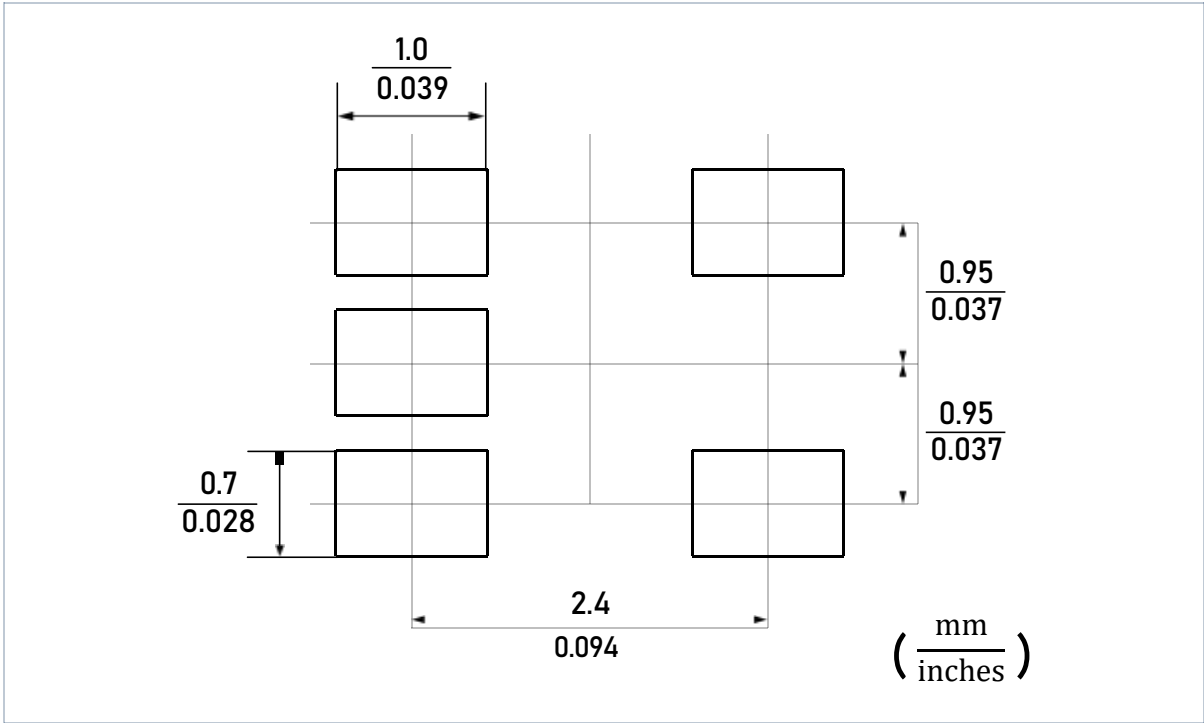
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTP842-33QT5/R6	SOT23	5	3 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTP842-33RQT5/R6	SOT23	5	3 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTP842-AEQV8/R6	EMSOP	8	3 000	330	12.5	5.0	3.5	2.0	8.0	12.0	Q1
LTP842-AEQS8/R8	ESOP	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1

Package Dimension

DIMENSIONS, SOT23-5L

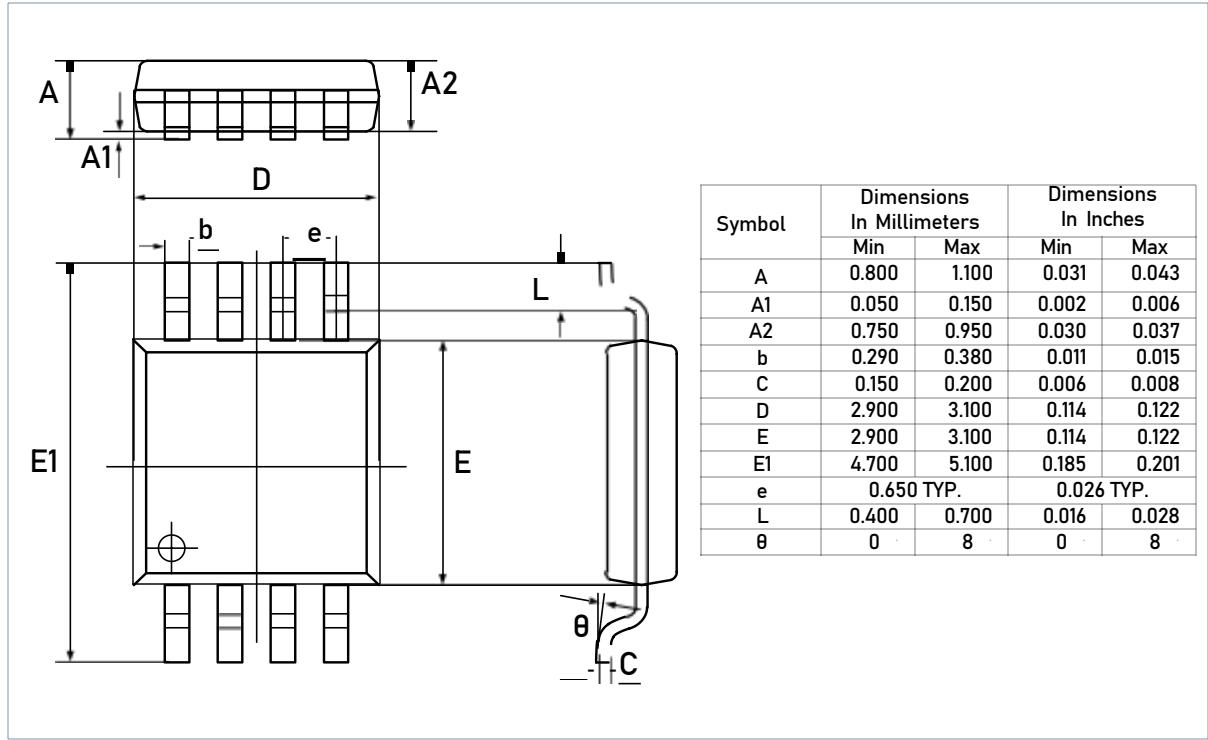


RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L

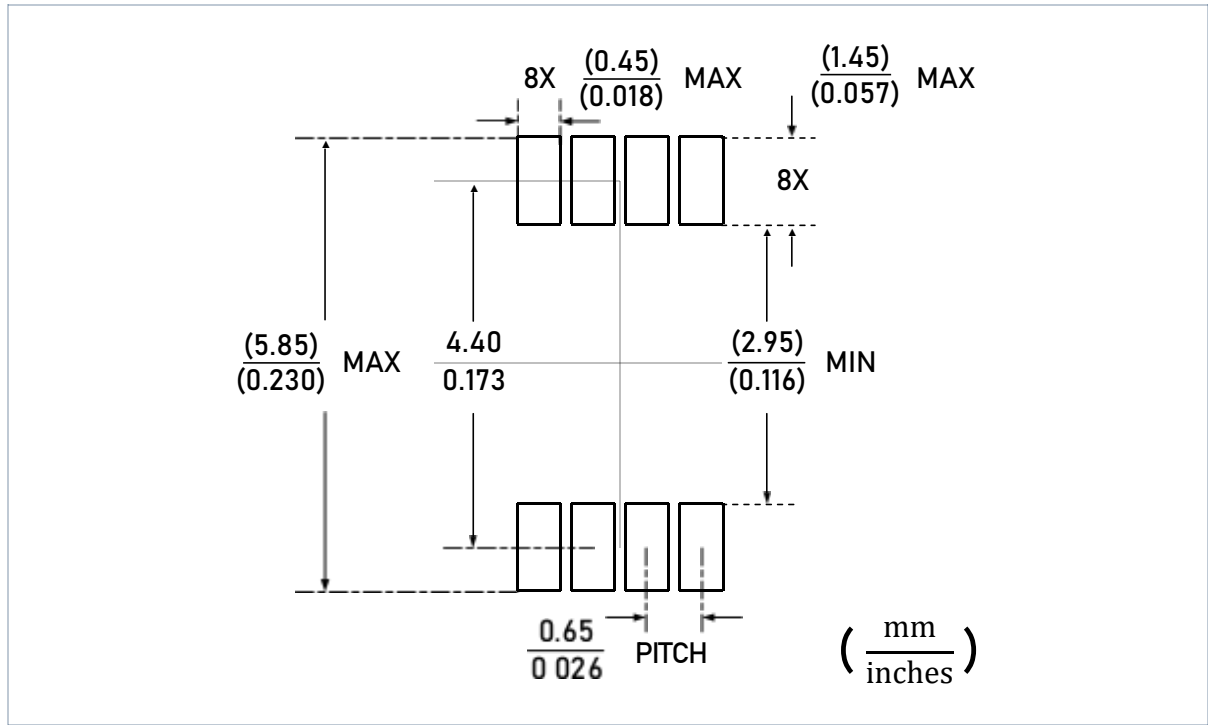


Package Dimension (Cont.)

DIMENSIONS, EMSOP-8L



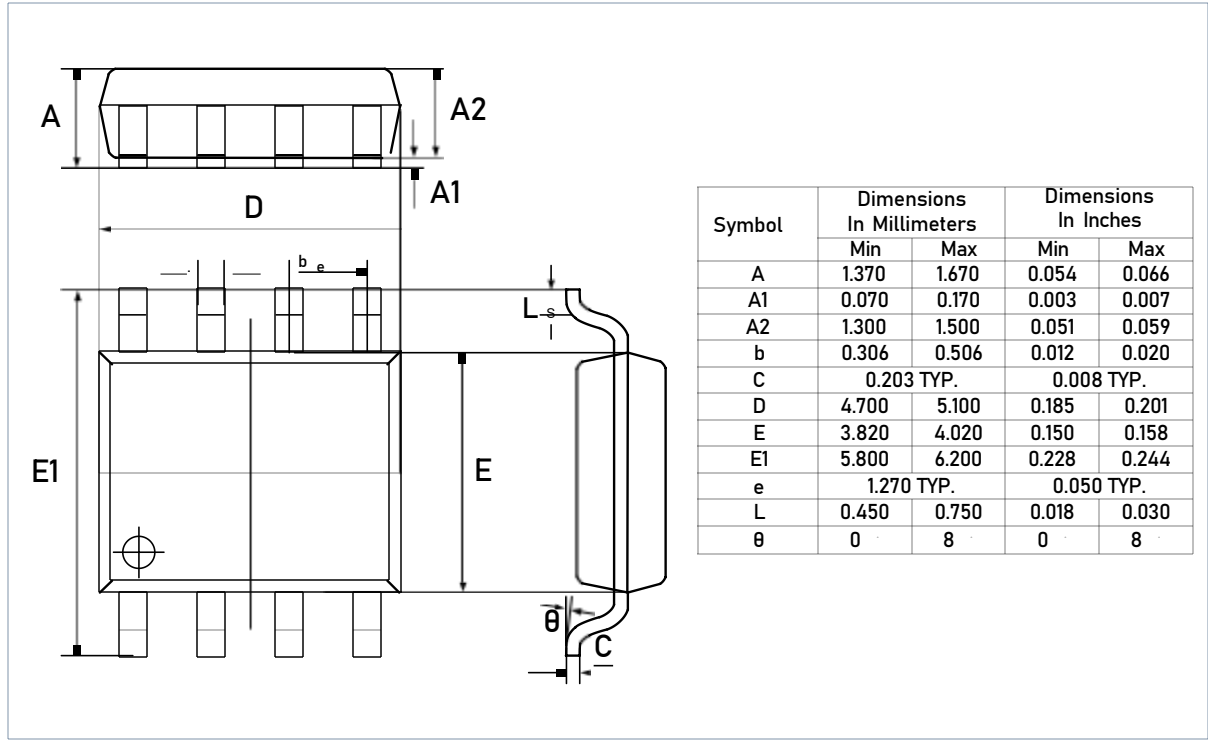
RECOMMENDED SOLDERING FOOTPRINT, EMSOP-8L



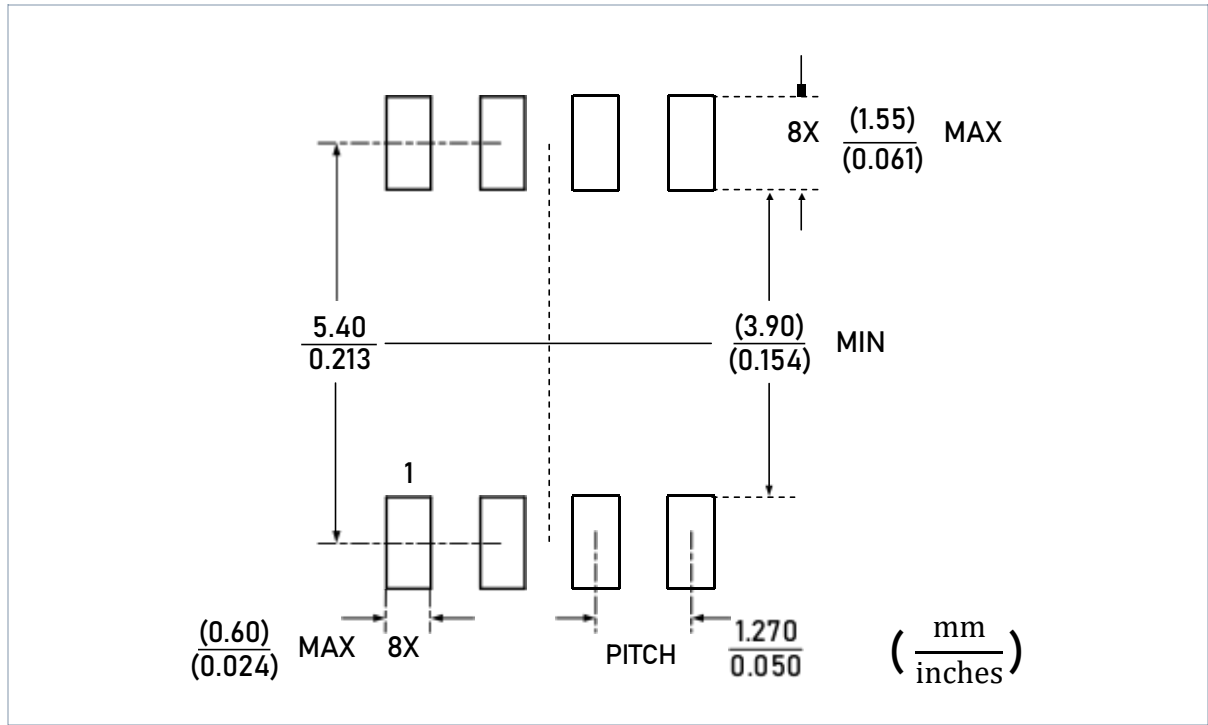
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Package Dimension (Cont.)

DIMENSIONS, ESOP-8L



RECOMMENDED SOLDERING FOOTPRINT, ESOP-8L



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