LTC725, LTC726, LTC727, LTC728

Precision, 11MHz, Low-Noise, RRIO, CMOS Amplifiers

General Description

The LTC72x family of single-, dual- and quad-channel operational amplifiers represent a new generation of general-purpose, low-power op-amps. Featuring rail-to-rail input and output (RRIO) swings, low quiescent current (typical 720µA) combined with a wide bandwidth (11MHz) and very low noise (8nV/√Hz at 1kHz) makes this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance, such as audio outputs, motor phase current sensing, photodiode amplification, barcode scanners and white goods. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the LTC72x amplifiers provides ease-of-use to the circuit designer: unity gain stability with capacitive loads of up to 300pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions and high electro-static discharge (ESD) protection (4kV HBM). The LTC72x amplifiers are optimized for operation at voltages as low as +1.8V (±0.9V) and up to +5.5V(±2.75V) at the temperature range of 0°C to 70°C and operation at voltages from +2.0V (±1.0V) to +5.5V (±2.75V) over the extended temperature range of -40°C to +125°C.

The LTC725 (single) is available in SOT23-5L and SC70-5L packages. The LTC726 (dual) is offered in SOIC-8L, MSOP-8L, TSSOP-8L and DFN2x2-8L packages. The LTC727 (single) is available in SOT23-5L and SC70-5L packages. The quad-channel LTC728 is offered in SOIC-14L, TSSOP-14L, QFN2x2-14L and QFN3x3-16L packages.

Features and Benefits

- Low Input Offset Voltage: ±0.35 mV Maximum
- Wide Unity-Gain Bandwidth: 11 MHz
- High Slew Rate: 11V/us
- Fast Settling: 0.26us to 0.1%
- Low Noise: 8nV/√Hz at 1kHz
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Single 1.8 V to 5.5 V Supply Voltage
- Low Supply Current: 720µA at 5.5V Supply Per Amplifier
- Extended Temperature Range: -40°C to +125°C

Applications

- HEV/EV inverter and motor control
- Battery-Powered Instruments
- On-board (OBC) and wireless charger
- ADAS
- Motor Phase Current Sense
- Sensor Signal Conditioning

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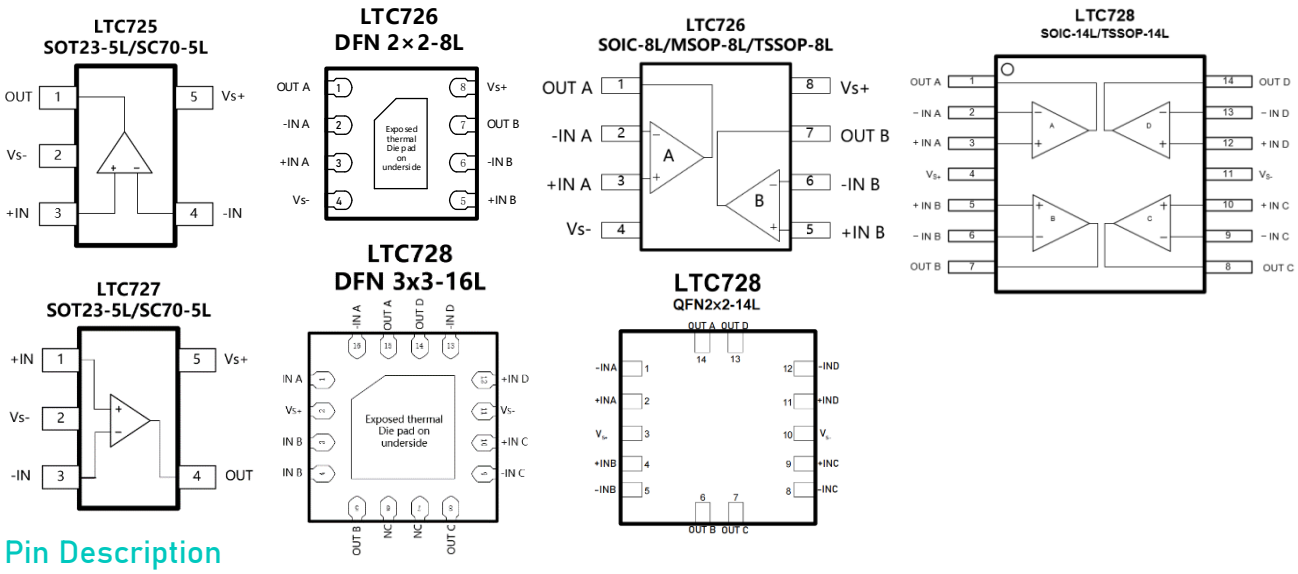
Pin Configurations (Top View)



Pin Description

Symbol	Description
-IN	inverting input of the amplifier. The voltage range is from (V_{S-} – 0.1V) to (V_{S+} + 0.1V).
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as -IN.
V_{S+}	Positive power supply.
V_{S-}	Negative power supply.
OUT	Amplifier output.

Ordering Information

Type Number	Package Name	Package Quantity	Marking Code (1)
LTC725XT5/R6	SOT23-5L	Tape and Reel, 3 000	AH1I
LTC725XC5/R6	SC70-5L	Tape and Reel, 3 000	AH1I, H5
LTC726XS8/R8	SOIC-8L	Tape and Reel, 4 000	AH2IX
LTC726XV8/R6	MSOP-8L	Tape and Reel, 3 000	AH2T
LTC726XT8/R8	TSSOP-8L	Tape and Reel, 4 000	AH2T
LTC726XF8/R6	DFN2x2-8L	Tape and Reel, 3 000	AH2T
LTC727XT5/R6	SOT23-5L	Tape and Reel, 3 000	AH3I
LTC727XC5/R6	SC70-5L	Tape and Reel, 3 000	H7
LTC728XS14/R5	SOIC-14L	Tape and Reel, 2 500	AH4IX
LTC728XT14/R6	TSSOP-14L	Tape and Reel, 3 000	AH4IX
LTC728XF14/R6	QFN2x2-14L	Tape and Reel, 3 000	AH4I
LTC728XF16/R10	QFN3x3-16L	Tape and Reel, 5 000	AH4T, AN4T

(1) There may be multiple device markings, a varied marking character of "x", or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

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Limiting Value -In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	10.0 V
Signal Input Terminals: Voltage, Current	V_{S-} – 0.5 V to V_{S+} + 0.5 V, ±10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	–65 °C to +150 °C
Junction Temperature, T_J	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

ESD Ratings

Parameter	Item	Level	UNIT
Electrostatic Discharge Voltage	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	4 000	V
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	2 000	

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Electrical Characteristics

V_S = 5.0 V, T_A = + 25 °C, V_{CM} = V_S/2, V_O = V_S /2, and R_L = 10 kΩ connected to V_S/2, unless otherwise noted.

Boldface limits apply over the specified temperature range, T_A = -40 to +125°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			±0.1	±0.35	mV
		T_A = -40 to +125 °C			±0.5	
Offset voltage drift	V_{OS} TC	T_A = -40 to +125 °C		±1	±3	µV/°C
Power supply rejection ratio	PSRR	V_S = 2.0 to 5.5 V, V_{CM} < V_{S+} -2 V	95	110		dB
		T_A = -40 to +125 °C	82			
INPUT BIAS CURRENT						
Input bias current	I_B			1		pA
		T_A = +85 °C		150		
		T_A = +125 °C		500		
Input offset current	I_{OS}			1		pA
NOISE						
Input voltage noise	V_n	f = 0.1 to 10 Hz		3.7		$µV_{P-P}$
Input voltage noise density	e_n	f = 1 kHz		8		nV/√Hz
Input current noise density	I_n	f = 1 kHz		5		fA/√Hz
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}		V_{S-} - 0.1		V_{S+} + 0.1	V
Common-mode rejection ratio	CMRR	V_S = 5.5 V, V_{CM} = -0.1 to 3.5 V	70	96		dB
		V_{CM} = 0 to 3.3 V, T_A = -40 to +125 °C	65			
		V_S = 5.5 V, V_{CM} = 4.5 to 5.6 V	66	93		
		V_{CM} = 4.5 to 5.5V, T_A = -40 to +125 °C	62			
INPUT IMPEDANCE						
Input capacitance	C_{IN}	Differential		2.0		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{VOL}	R_L = 10 kΩ, V_O = 0.05 to 3.5 V	93	100		dB
		T_A = -40 to +125 °C	87			
		R_L = 2kΩ, V_O = 0.15 to 3.5 V	88	96		
		T_A = -40 to +125 °C	75			
FREQUENCY RESPONSE						
Gain bandwidth product	GBW			11		MHz
Slew Rate	SR	G = +1, C_L = 100 pF, V_O = 1.0 to 4.0 V		11		V/µs
Total harmonic distortion+ noise	THD+N	G = +1, f = 1 kHz, V_O = 0.5 V_{RMS}		0.0005		%

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Electrical Characteristics (Cont.)

V_S = 5.0 V, T_A = + 25 °C, V_{CM} = V_S/2, V_O = V_S /2, and R_L = 10 kΩ connected to V_S/2, unless otherwise noted.

Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Settling time	t_S	To 0.1%, G = +1, 1V step		0.26		µs
		To 0.01%, G = +1, 1V step		0.34		
Overload recovery time	t_{OR}	V_{IN} x Gain > V_S		0.3		µs
OUTPUT						
High output voltage swing	V_{OH}	R_L = 10 kΩ	V_{S+} -11	V_{S+} - 8		mV
		R_L = 600 Ω	V_{S+} - 172	V_{S+} - 128		
Low output voltage swing	V_{OL}	R_L = 10 kΩ		V_{S-} +5	V_{S-} +7	mV
		R_L = 600 Ω		V_{S-} +80	V_{S-} +110	
Short- circuit current	I_{SC}			+90/ −70		mA
POWER SUPPLY						
Operating supply voltage	V_S	T_A = 0 to +70 °C	1.8		5.5	V
		T_A = -40 to +125 °C	2.0		5.5	
Quiescent current (per amplifier)	I_Q	V_S = 2.0 V		570	780	µA
		V_S = 5.5 V		720	990	
THERMAL CHARACTERISTICS						
Operating temperature range	T_A		-40		+125	°C
Package Thermal Resistance	θ_{JA}	SOT23-5L		190		°C/W
		SC70-5L		333		
		SOIC-8L		125		
		MSOP-8L		201		
		TSSOP-8L		160		
		DFN2x2-8L		94		
		SOIC-14L		115		
		TSSOP-14L		112		
		QFN2x2-14L		87		
		QFN3x3-16L		65		

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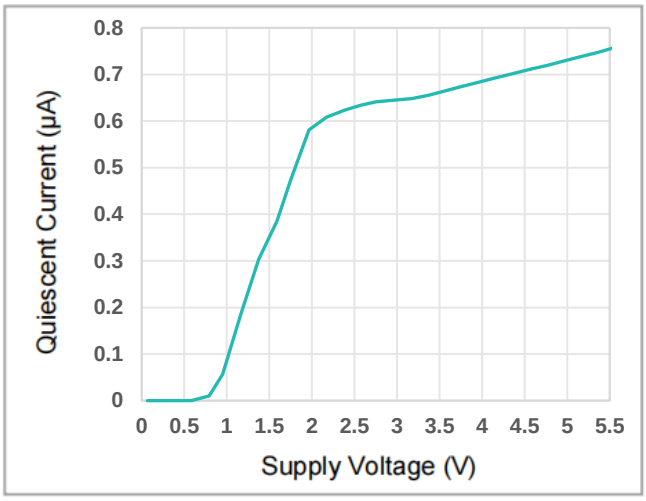
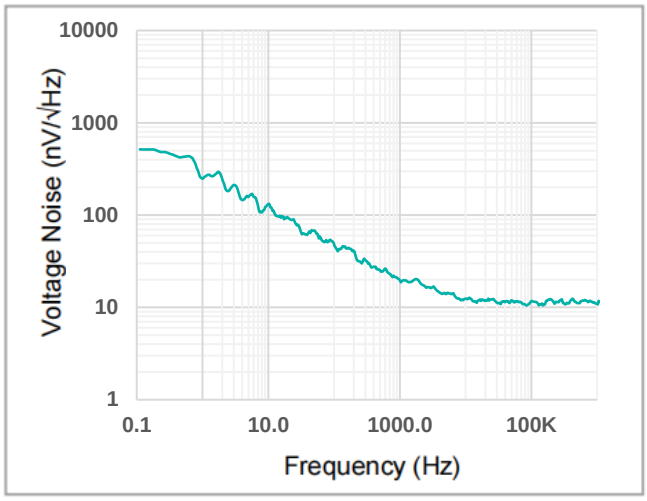
Typical Performance Characteristics

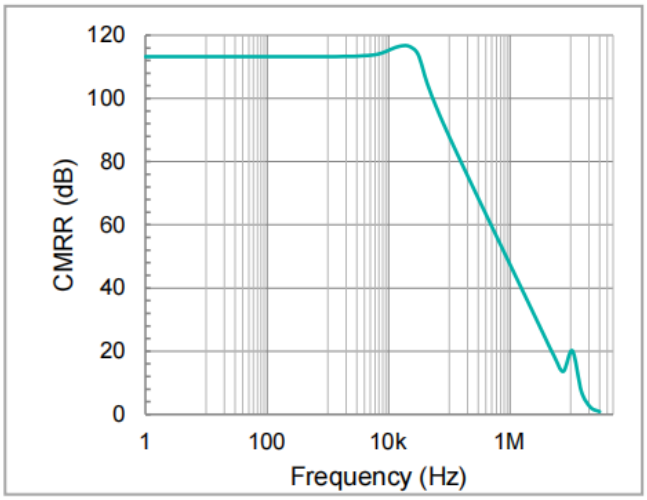
At T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2 and R_L = 10 kΩ connected to V_S / 2, unless otherwise noted.



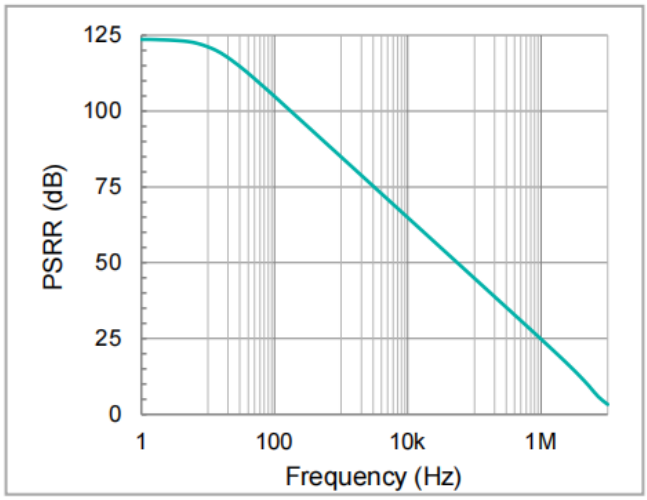
Quiescent Current as a function of Supply Voltage.



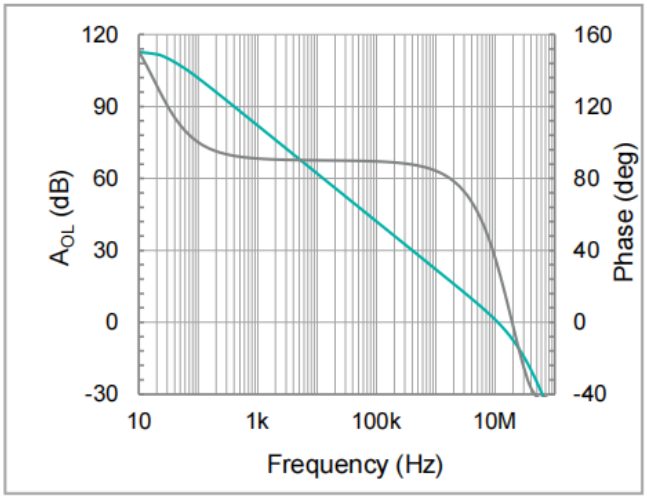
Input Voltage Noise Spectral Density as a function of Frequency.



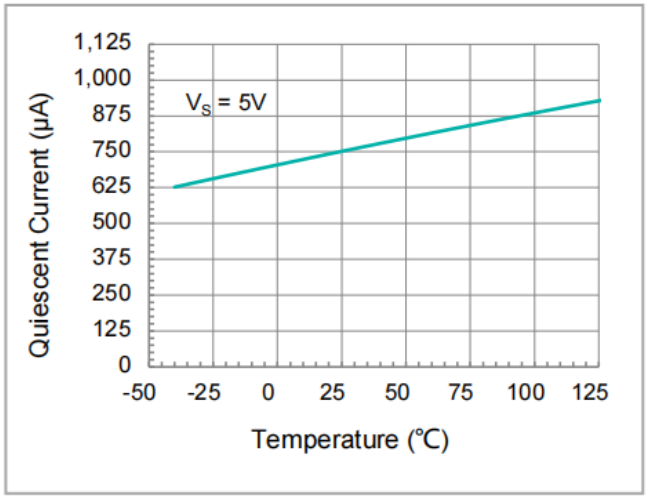
Common-mode Rejection Ratio as a function of Frequency.



Power Supply Rejection Ratio as a function of Frequency.



Open-loop Gain and Phase as a function of Frequency.



Quiescent Current as a function of Temperature.

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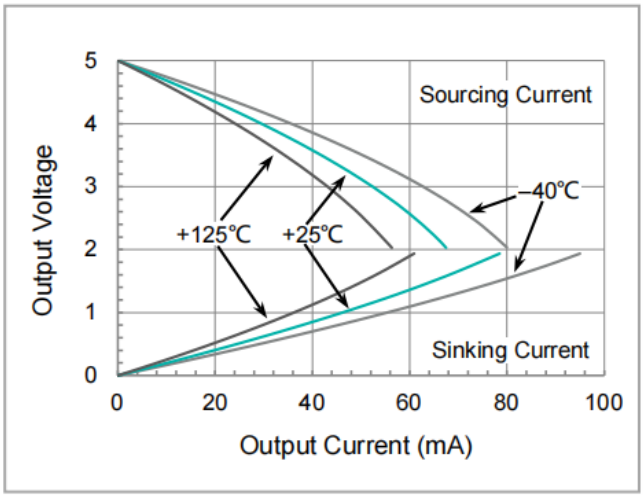
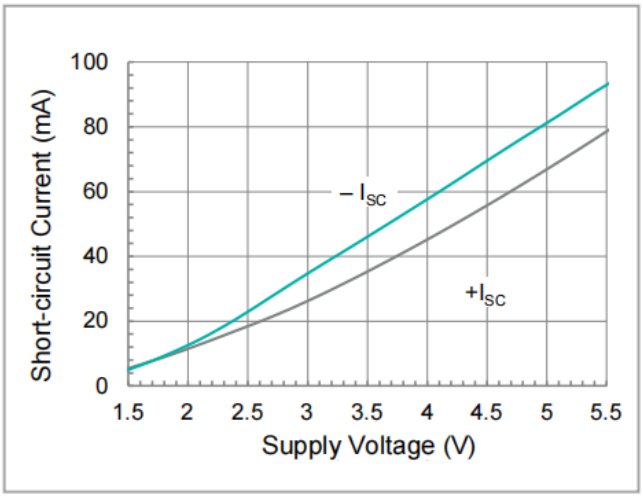
Typical Performance Characteristics (Cont.)

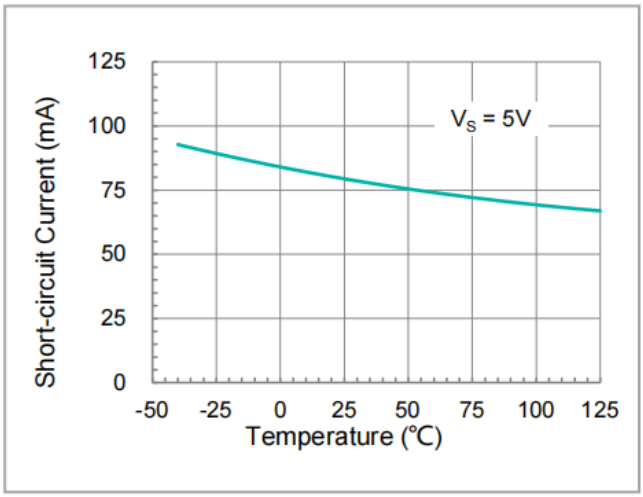
At T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2 and R_L = 10 kΩ connected to V_S / 2, unless otherwise noted.



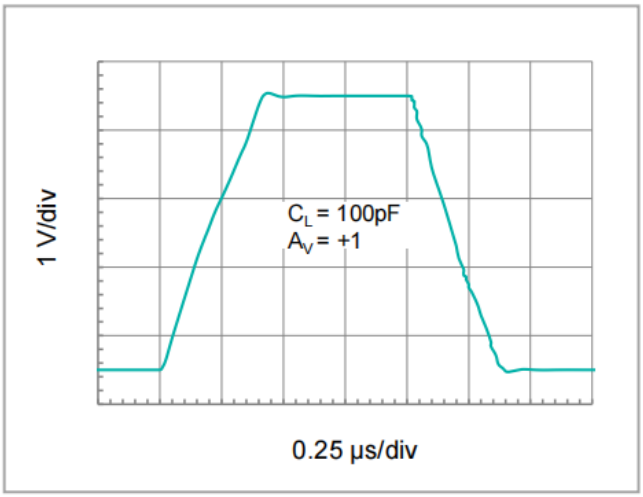
Output Voltage Swing as a function of Output Current.



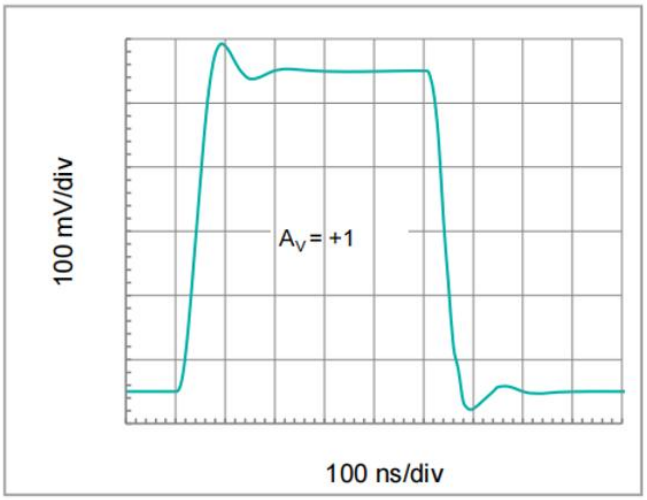
Short-circuit Current as a function of Supply Voltage.



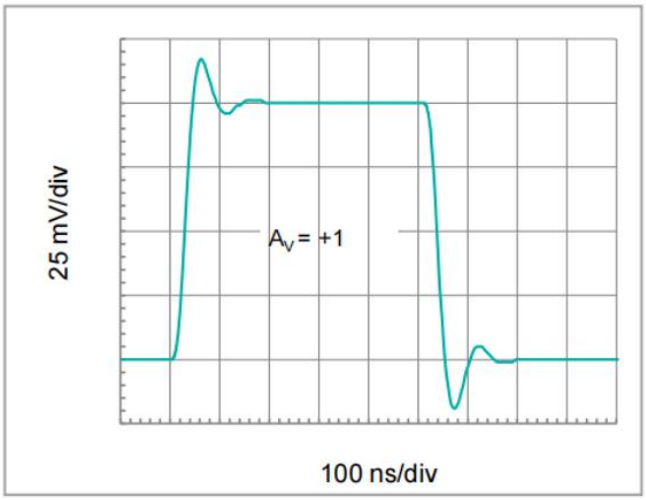
Short-circuit Current as a function of Temperature.



Large Signal Step Response.



Small Signal Step Response (500mV)



Small Signal Step Response (100mV)

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Application Notes

The LTC72x is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8V to 5.5V at the temperature range of 0°C to 70°C, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving≤10-kΩ loads connected to any point between V_{S+} and ground. The input common-mode voltage range includes both rails, and allows the LTC72x family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The LTC72x features 11-MHz bandwidth and 11 -V/µs slew rate with only 720-µA supply current per amplifier, providing good ac performance at very low power consumption. DC applications are also well served by the low input voltage noise of 8 nV/√Hz at 1 kHz, low input bias current, and low input offset voltage. The maximum input offset voltage is ±0.35 mV at TA = 25°C and ±0.5 mV over the temperature range of −40°C to +125°C. The input offset voltage drift is typically ±1 µV/°C, with a maximum of ±3 µV/°C.

OPERATING VOLTAGE

The LTC72x family is optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V(±2.75 V) at the temperature range of 0 °C to 70 °C and fully specified and ensured for operation from2.0 V to 5.5 V (±1.0 V to ±2.75 V). In addition, many specifications apply from − 40 °C to +125 °C. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

NOTE: Supply voltages (V_{S+} to V_{S-}) higher than +10 V can permanently damage the device.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the LTC72x series extends 100-mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+} − 1.4 V to the positive supply, whereas the P-channel pair is active for inputs from 100-mV below the negative supply to approximately V_{S+} − 1.4 V. There is a small transition region, typically V_{S+} − 1.2 V to V_{S+} − 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200-mV with process variation. Thus, the transition region (both stages on) can range from V_{S+} − 1.4 V to V_{S+} − 1.2 V on the low end, up to V_{S+} − 1V to V_{S+} − 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the LTC72x during normal operation is approximately 1-pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

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INPUT EMI FILTER AND CLAMP CIRCUIT

Figure 1 shows the input EMI filter and clamp circuit. The LTC72x op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500-mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to ±10-mA as stated in the Absolute Maximum Ratings.

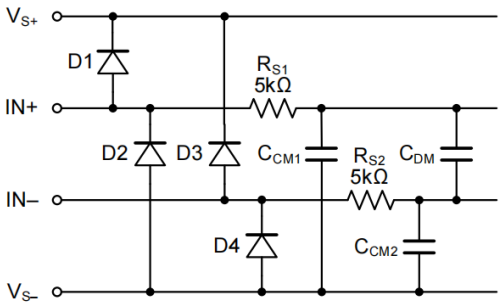

Figure 1: Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the LTC72x family is composed of two 5-kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}),and a differential capacitor (C_{DM}). These RC networks set the −3 dB low-pass cutoff frequencies at 35-MHzfor common-mode signals, and at 22-MHz for differential signals

RAIL-TO-RAIL OUTPUT

Designed as a micro-power, low-noise operational amplifier, the LTC72x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 100-kΩ, the output swings typically to within 5-mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 600-Ω, the output swings typically to within 125-mV of the positive supply rail and within 90-mV of the negative supply rail.

CAPACITIVE LOAD AND STABILITY

The LTC72x family can safely drive capacitive loads of up to 300-pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the LTC72x op-amps must drive a load exceeding 300-pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 2. R_{ISO} isolates the amplifier output and feedback

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network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} for ms a voltage divider with the R_L.

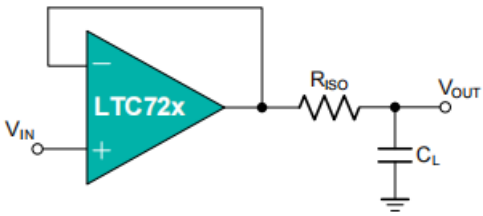

Figure 2: Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 3. It provides DC accuracy as well as AC stability. The RF provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input there by preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, o(b) by placing a capacitor in parallel with the feedback resistor to counter ac the parasitic capacitance associated with inverting node.

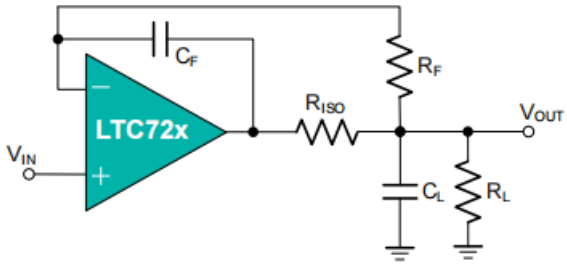

Figure 3: Indirectly Driving Heavy Capacitive Load with DC Accuracy

OVERLOAD RECOVERY

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the LTC72x family is approximately 0.3-µs.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pin-the non-inverting input, inverting input, positive supply, negative supply, and output pins—are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

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The LTC72x op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN_PEAK} / \Delta V_{OS})$$

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the LTC72x op-amps, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure4 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon stand off insulators.

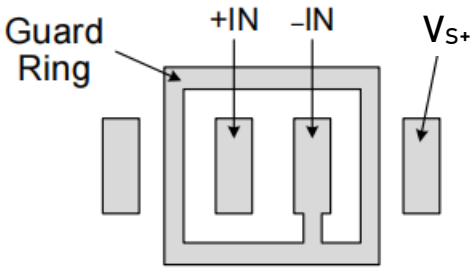

Figure 4: Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup

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Typical Application Circuit

Active filter

The LTC72x family is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 5 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cut-off frequency, roll-off is －40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

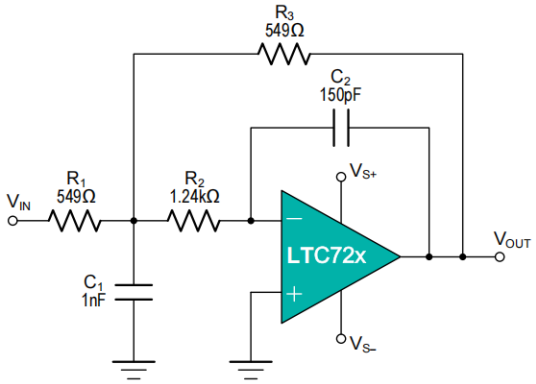

Figure 5: Second-Order, Butterworth, 500-kHz Low-Pass Filter

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a non-inverting output can be achieved through one of these options:

1. adding an inverting amplifier;

2.adding an additional second-order MFB stage;

3.using a non-inverting filter topology, such as the Sallen-Key (shown in Figure 6)

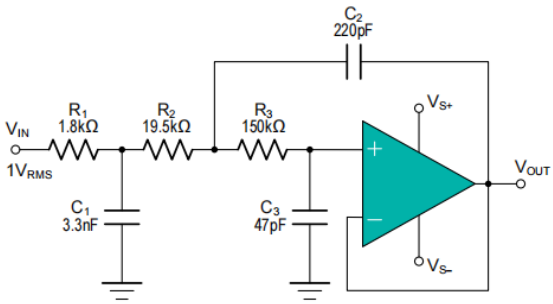

Figure 6: Configure das a Three-Pole, 20-kHz, Sallen-Key Filter

MOTOR PHASE CURRENT SENSING

The current sensing amplification shown in Figure 7 has a slew rate of $\pi f V_{P-P}$ for the output of sine wave signal, and has a slew rate of $2fV_{PP}$ for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10 kHz to 20 kHz, and one cycle time is 100 μs for a 10 kHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the Figure 7 shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (t_{SR}) due to the op-amp's slew rate, and the measurement settling time (t_{SET}). For a 2-shunt solution of motor phase current sensing, if the minimum duty cycle of the PWM is defined at 5%, and the t_{SR} is required

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at 20% of a total time window for a phase current monitoring, in case of a 3.3 V motor control system (3.3 V MCU with 12-bit ADC), the op amp's slew rate should be more than:

3.3V/(100µs×5%×20%)=3.3V/µs

At the same time, the op-amp's bandwidth should be much greater than the PWM frequency, like 10 time at least.

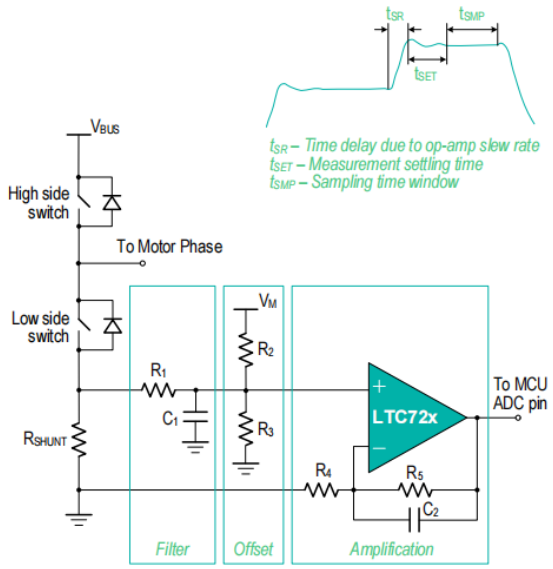

Figure 7: Current Shunt Monitor Circuit

DIFFERENTIAL AMPLIFIER

The circuit shown in Figure 8 performs the difference function. If the resistors ratios are equal R4/R3= R2/R1, then:

$V_{OUT}=(V_p-V_n)\times R_2/R_1+V_{REF}$

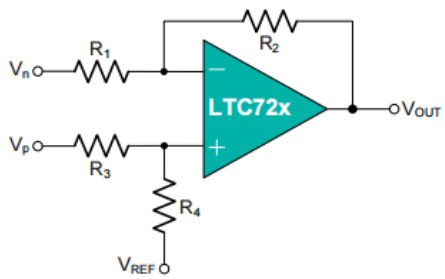

Figure 8: Differential Amplifier

INSTRUMENTATION AMPLIFIER

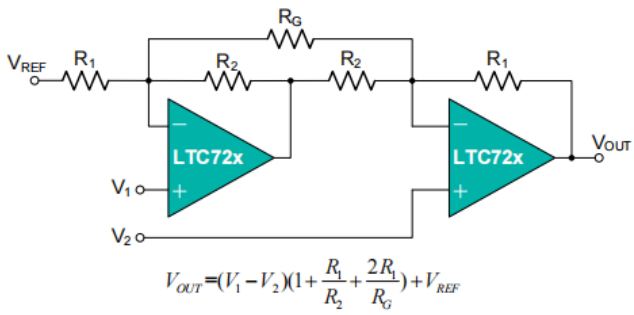

Figure 9: Instrumentation Amplifier

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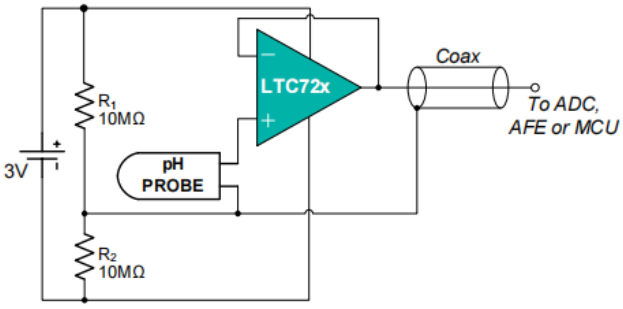
The LTC72x family is well suited for conditioning sensor signals in battery-powered applications. Figure 9 shows a two op-amp instrumentation amplifier, using the LTC72x op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, the V_{REF} is typically $V_S/2$.

BUFFERED CHEMICAL SENSORS



All components contained within the pH probe

Figure 10: Buffered pH Probe

The LTC72x family has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors, such as pH probes. As an example, the circuit in Figure 10 eliminates expansive low-leakage cables that that is required to connect a pH probe (general purpose combination pH probes, e.g Corning 476540) to metering ICs such as ADC, AFE and/or MCU. A LTC72x op-amp and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry the op-amp's output signal to subsequent ICs for pH reading.

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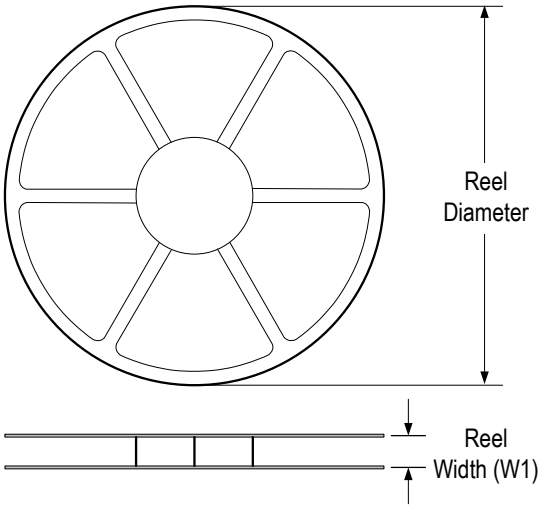
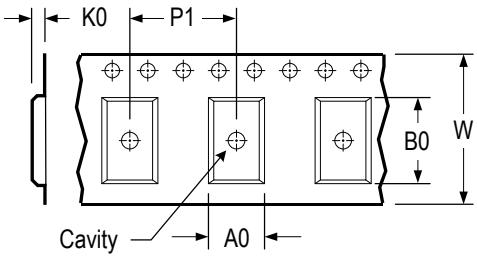
Tape and Reel Information

REEL DIMENSIONS

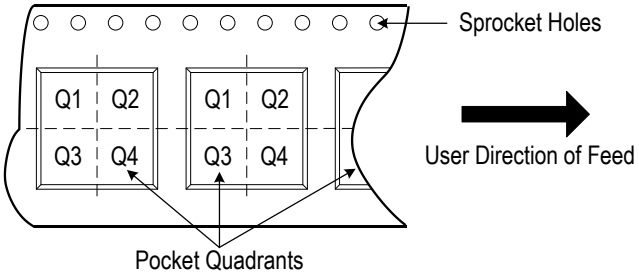


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE



* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTC725XT5/R6	SOT23	5	3 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTC725XC5/R6	SC70	5	3 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTC726XS8/R8	SOIC	8	4 000	330	12.5	6.6	5.3	2.0	8.0	12.0	Q1
LTC726XV8/R6	MSOP	8	3 000	330	12.5	5.0	3.5	2.0	8.0	12.0	Q1
LTC726XT8/R8	TSSOP	8	4 000	330	12.5	6.5	4.0	1.2	8.0	12.0	Q1
LTC726XF8/R6	DFN2x2	8	3 000	178	9.5	2.25	2.25	1.0	4.0	8.0	Q1
LTC727XT5/R6	SOT23	5	3 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTC727XC5/R6	SC70	5	3 000	178	9.5	3.3	3.2	1.5	4.0	8.0	Q3
LTC728XS14/R5	SOIC	14	2 500	330	16.5	6.5	9.5	2.0	8.0	16.0	Q1
LTC728XT14/R6	TSSOP	14	3 000	330	16.5	6.9	5.5	1.3	8.0	16.0	Q1
LTC728XF14/R6	QFN2x2	14	3 000	178	9.5	2.25	2.25	0.8	4.0	8.0	Q1
LTC728XF16/R10	QFN3x3	16	5 000	330	12.5	3.5	3.5	1.2	8.0	12.0	Q1

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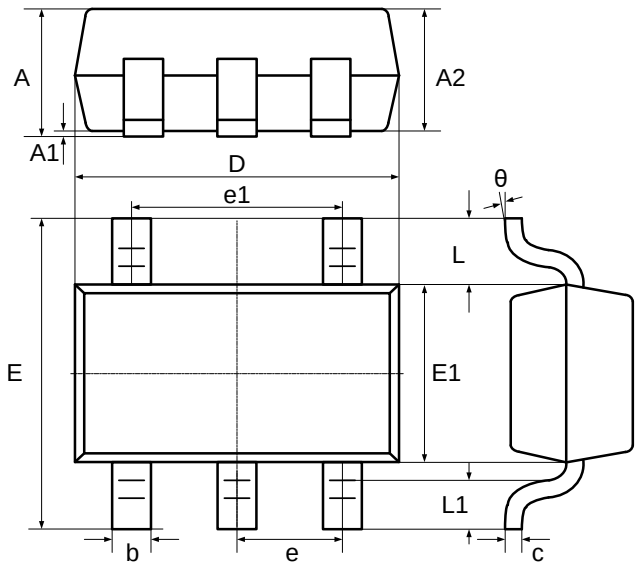
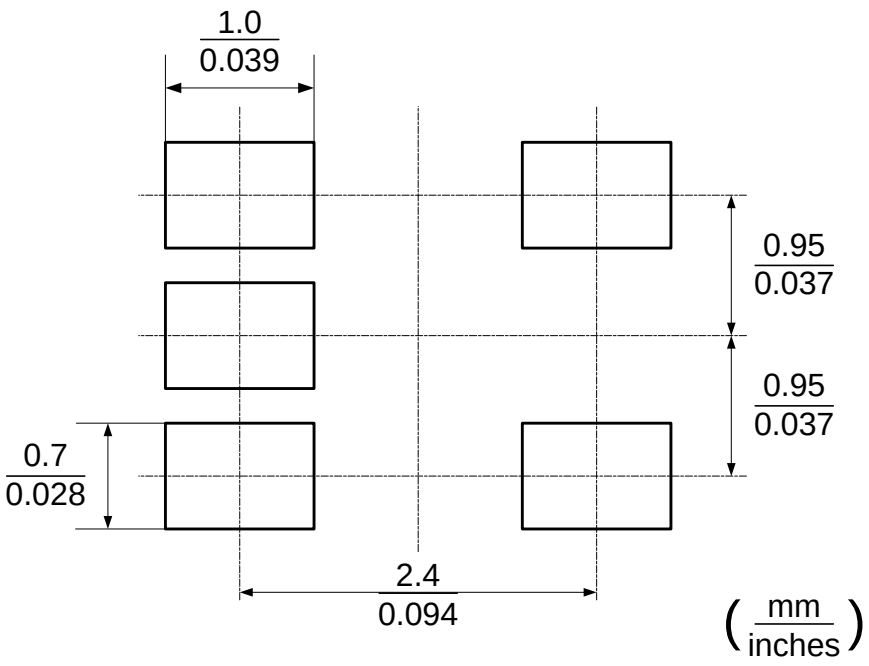
Package Outlines

DIMENSIONS, SOT23-5L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.25	-	0.049
A1	0.04	0.10	0.002	0.004
A2	1.00	1.20	0.039	0.047
b	0.33	0.41	0.013	0.016
c	0.15	0.19	0.006	0.007
D	2.820	3.02	0.111	0.119
E1	1.50	1.70	0.059	0.067
E	2.60	3.00	0.102	0.118
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.60 REF		0.024 REF	
L1	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



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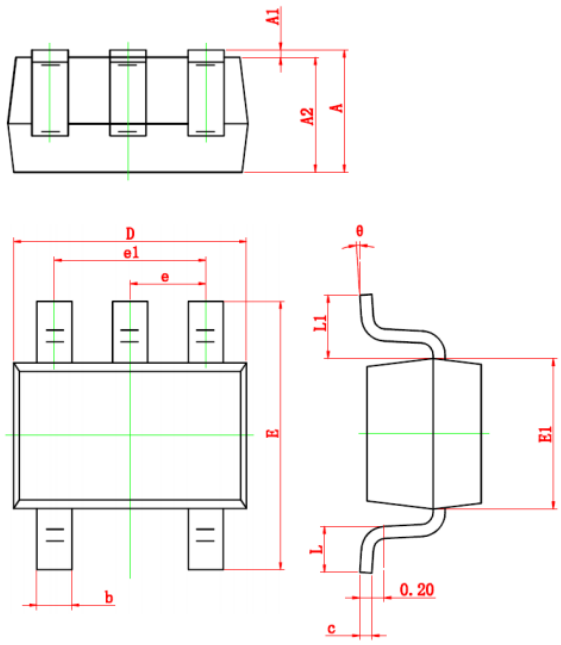
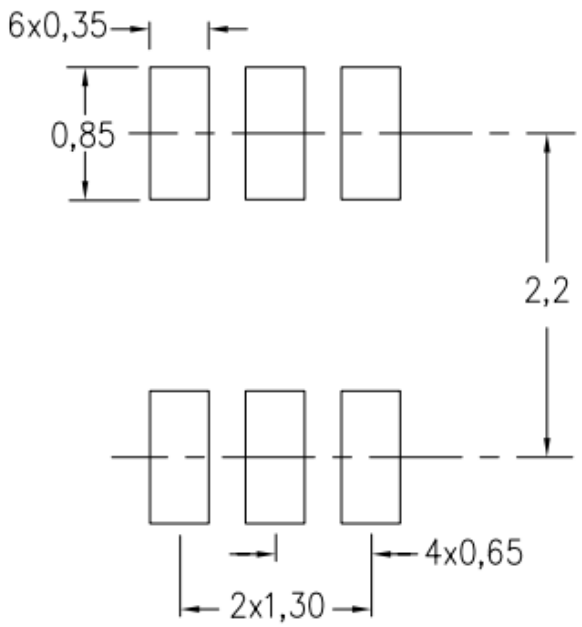
Package Outlines (Cont.)

DIMENSIONS, SC70-5L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650TYP		0.026REF	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525REF		0.021REF	
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SC70-5L



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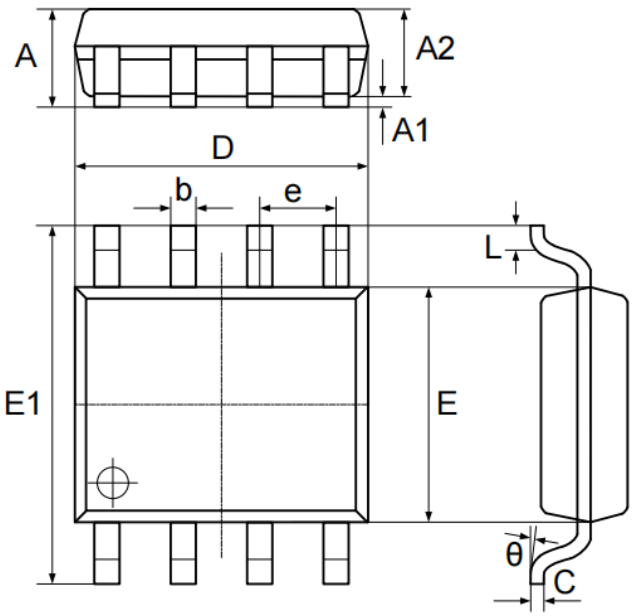
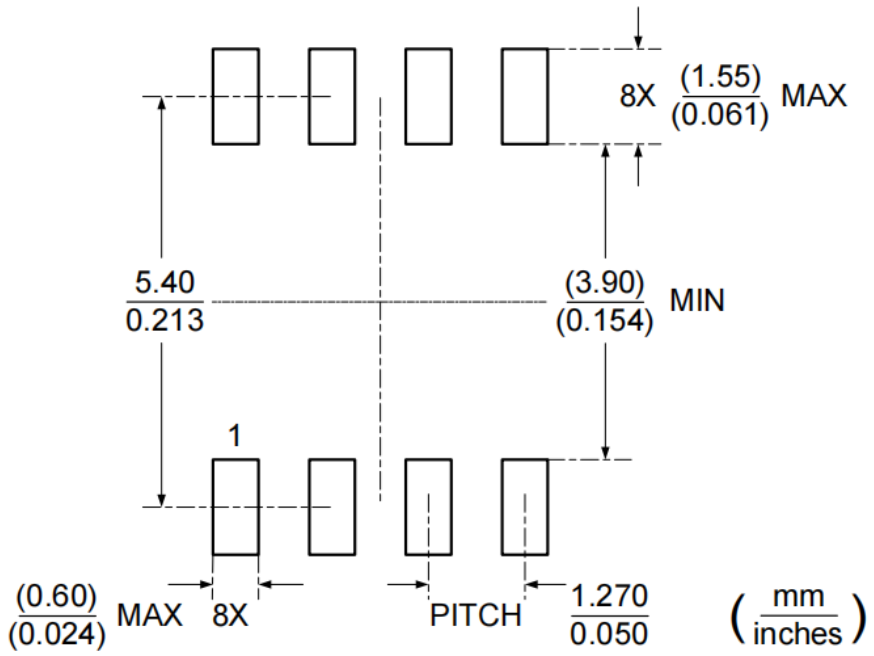
Package Outlines (Cont.)

DIMENSIONS, SOIC-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.054	0.066
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.051	0.059
b	0.306	0.506	0.012	0.020
C	0.203 TYP.		0.008 TYP.	
D	4.700	5.100	0.185	0.201
E	3.820	4.020	0.150	0.158
E1	5.800	6.200	0.228	0.244
e	1.270 TYP.		0.050 TYP.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



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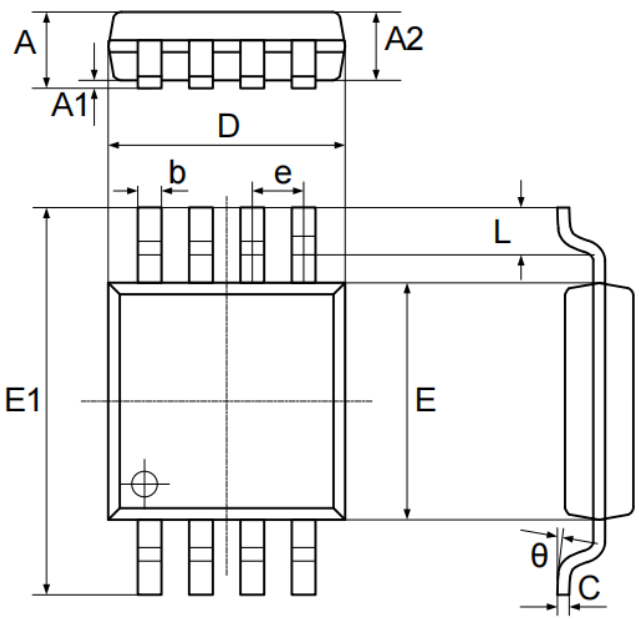
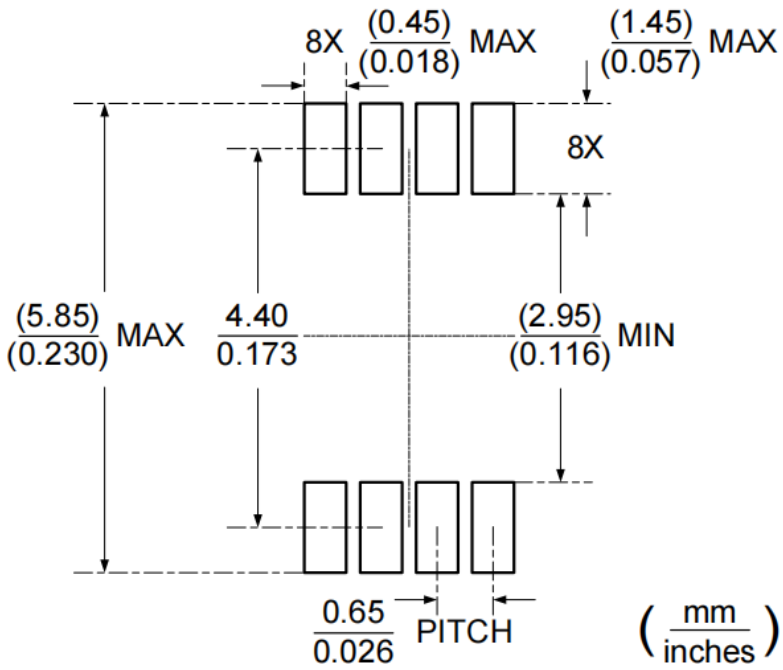
Package Outlines (Cont.)

DIMENSIONS, MSOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.290	0.380	0.011	0.015
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650 TYP.		0.026 TYP.	
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



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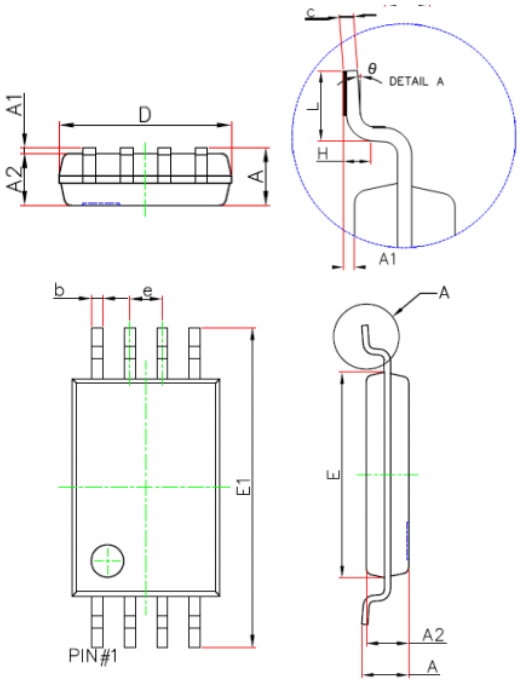
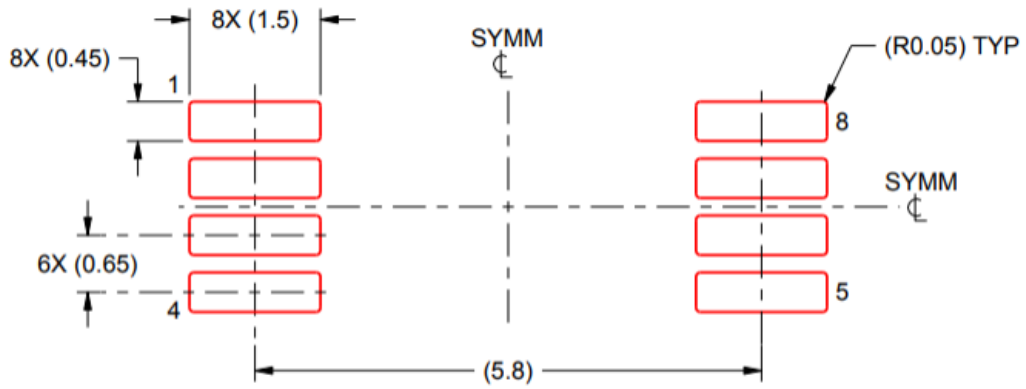
Package Outlines (Cont.)

DIMENSIONS, TSSOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.9	3.1	0.114	0.122
E	4.3	4.5	0.169	0.177
b	0.19	0.3	0.007	0.012
c	0.09	0.2	0.004	0.008
E1	6.25	6.55	0.246	0.258
A	—	1.2	—	0.047
A2	0.8	1	0.031	0.039
A1	0.05	0.15	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.5	0.7	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

RECOMMENDED SOLDERING FOOTPRINT, TSSOP-8L



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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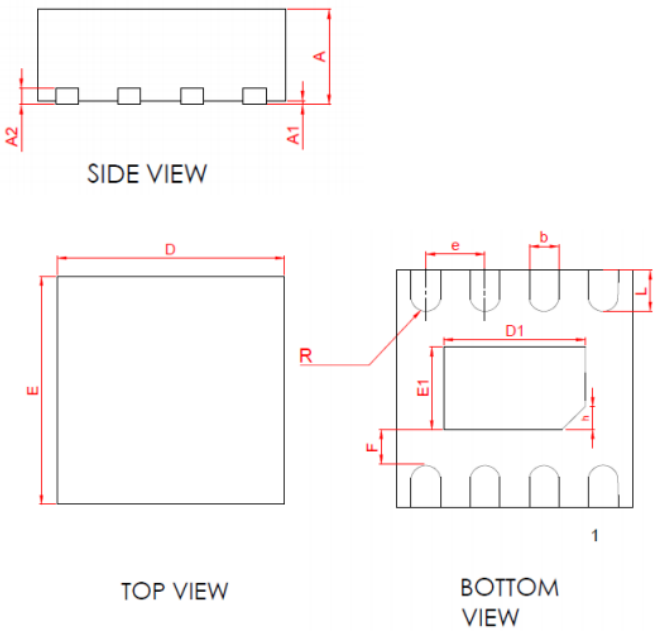
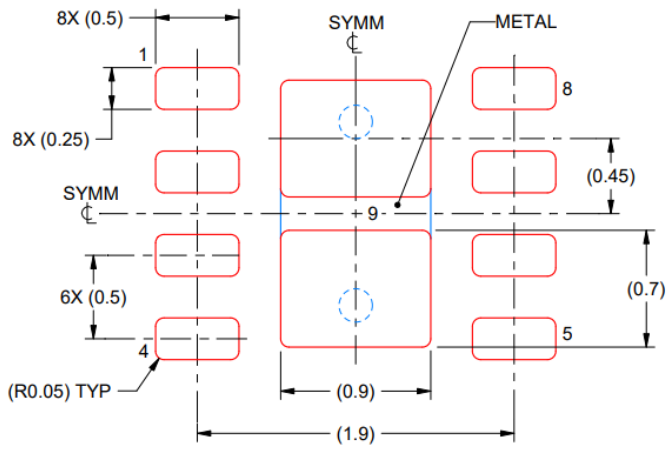
Package Outlines (Cont.)

DIMENSIONS, DFN2x2-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A2	0.200BSC		0.008	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E1	0.600	0.800	0.024	0.031
e	0.50REF		0.020	
L	0.300	0.400	0.012	0.016
F	0.250	0.350	0.010	0.014
h	REF0.18		0.007	

RECOMMENDED SOLDERING FOOTPRINT, DFN2x2-8L



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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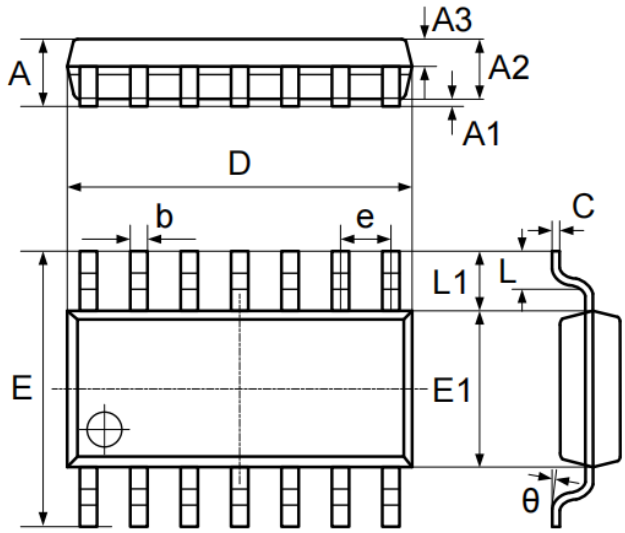
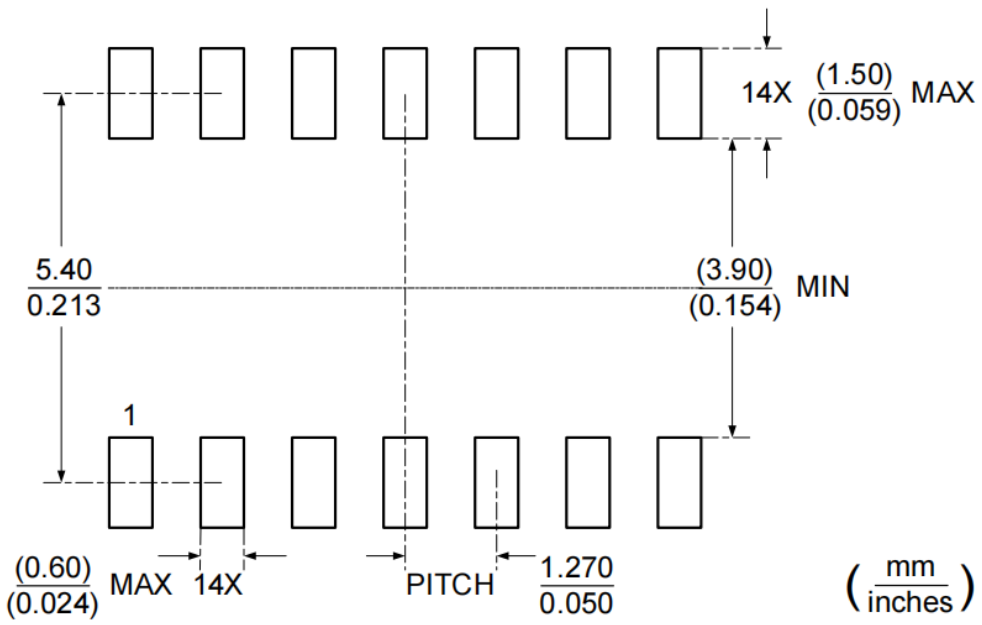
Package Outlines (Cont.)

DIMENSIONS, SOIC-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.057	0.073
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.053	0.061
A3	0.550	0.750	0.022	0.030
b	0.406 TYP.		0.016 TYP.	
C	0.203 TYP.		0.008 TYP.	
D	8.630	8.830	0.340	0.348
E	5.840	6.240	0.230	0.246
E1	3.850	4.050	0.152	0.159
e	1.270 TYP.		0.050 TYP.	
L1	1.040 REF.		0.041 REF.	
L	0.350	0.750	0.014	0.030
θ	2°	8°	2°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



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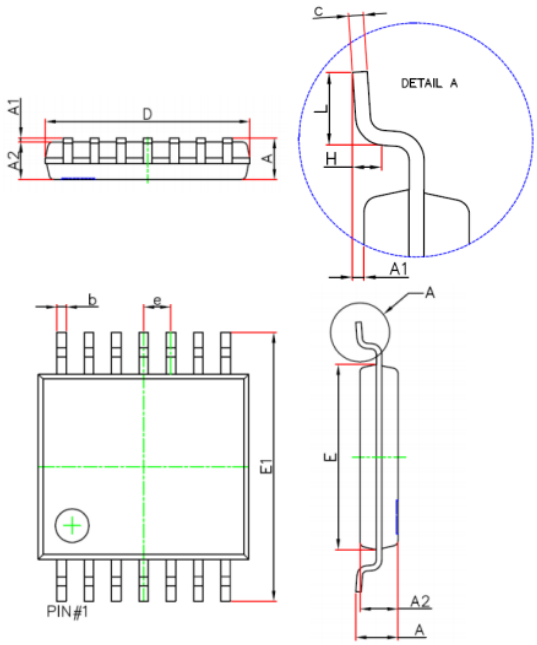
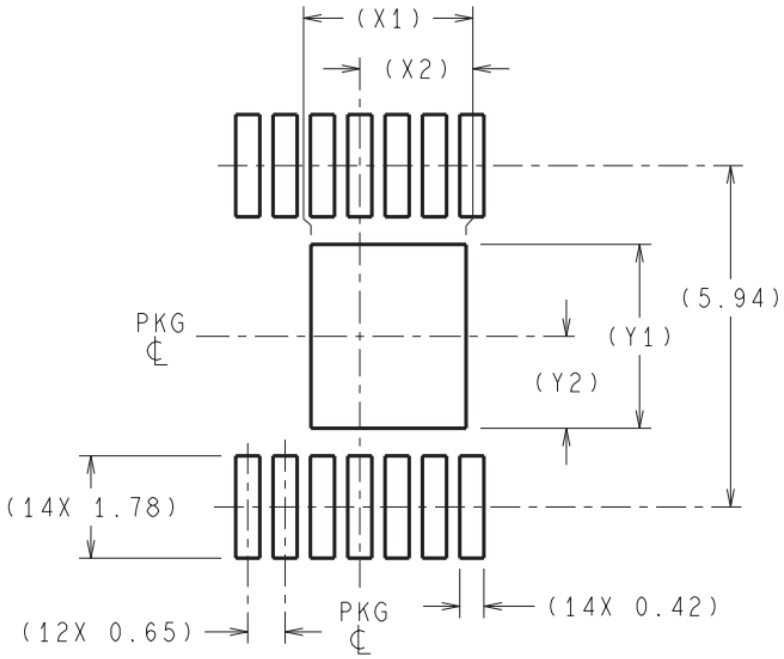
Package Outlines (Cont.)

DIMENSIONS, TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.9	5.1	0.193	0.201
E	4.3	4.5	0.169	0.177
b	0.19	0.3	0.007	0.012
c	0.09	0.2	0.004	0.008
E1	6.25	6.55	0.246	0.258
A	—	1.2	—	0.047
A2	0.8	1	0.031	0.039
A1	0.05	0.15	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.5	0.7	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L



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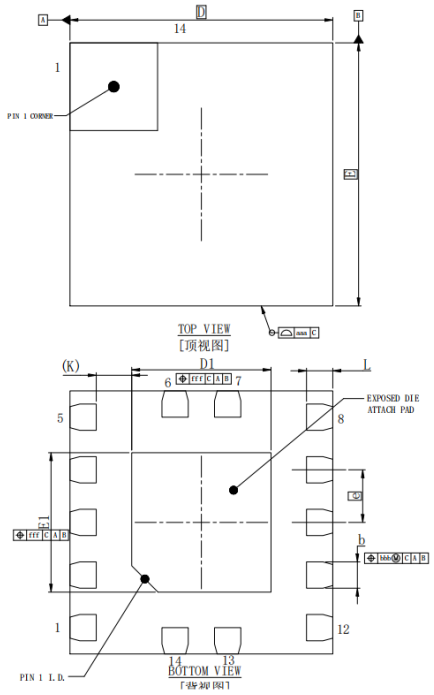
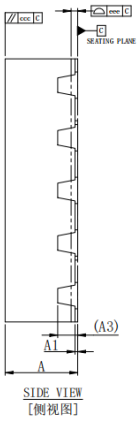
Package Outlines (Cont.)

DIMENSIONS, QFN2x2-14L





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.60
STAND OFF		A1	0	0.02	0.05
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D		2 BSC	
	Y	E		2 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D1	0.96	1.06	1.16
	Y	E1	0.96	1.06	1.16
LEAD LENGTH		L	0.10	0.20	0.30
LEAD TIP TO EP EDGE		K		0.27 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

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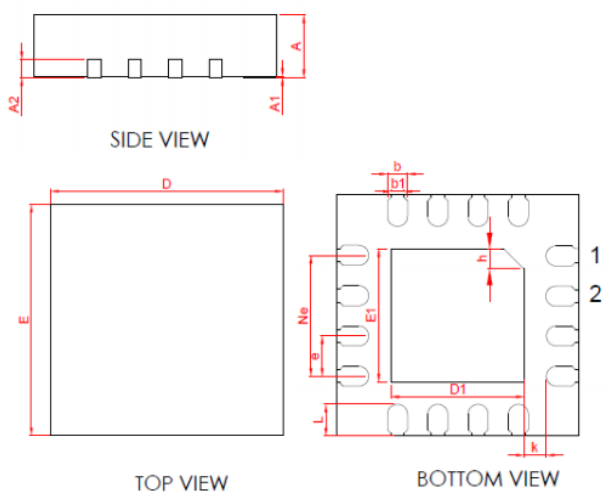
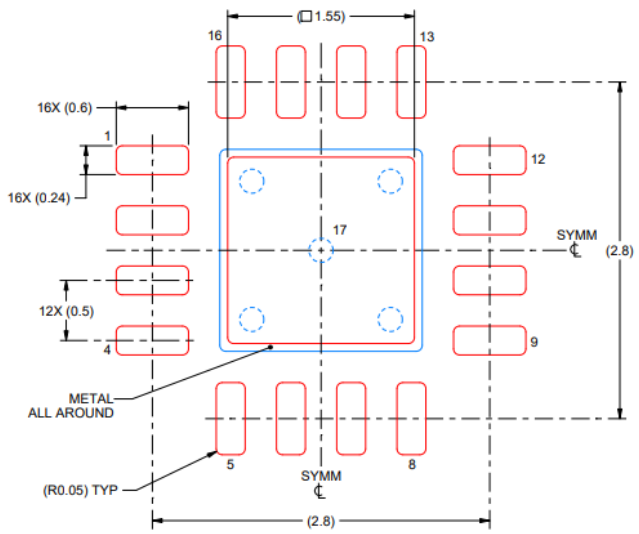
Package Outlines (Cont.)

DIMENSIONS, QFN3x3-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.16BSC		0.008	
A2	0.203BSC		0.008	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.700	0.063	0.067
E1	1.600	1.700	0.063	0.067
e	0.5BSC		0.020	
Ne	1.50BSC		0.020	
k	0.230	0.330	0.009	0.013
h	0.200	0.300	0.008	0.012
l	0.350	0.450	0.014	0.018

RECOMMENDED SOLDERING FOOTPRINT, QFN3x3-16L



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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For additional product information, or full data sheet, please contact with the Linearin's Sales Department or Representatives.

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